UNIVAC 9200

SPECIAL CONTROL ROUTINES
ESCR

SYS. S/N 2230 UNIT S/N

BOOK 1 OF 1

SPERRY RAND
UNIVAC
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SERVICING DOCUMENT MANUAL INDEX

MANUAL INDEX NO.			
PREFIX	TYPE NO.	SIZE	IND. VAR.
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SPECIFICATION APPROVAL SHEET

TITLE

NCF 9200 and/or 9300 INPUT/OUTPUT

Special Control Routine

ESCR

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APPROVAL H. B. Brown	12	12	68

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SPECIFICATION APPROVAL SHEET

SHEET 1-1b

TITLE

NCF 9200 and/or 9300 INPUT/OUTPUT
Special Control Routine
ESCR

COMPANY CONFIDENTIAL INFORMATION

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SPECIFICATION APPROVAL SHEET

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TITLE

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SPECIFICATION APPROVAL SHEET

SHEET 1-1d

TITLE

NCF 9200 and/or 9300 INPUT/OUTPUT

Special Control Routine

ESCR

COMPANY CONFIDENTIAL INFORMATION

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SH04479	A	—

CONTENTS

1. SCOPE

ESCR is a generalized, input/output control routine designed to minimize and facilitate the operations necessary to issue commands to any kind of device on the multiplexer and/or selector channels of NCF 9200 and 9300 computer systems. Subsequent termination status indications are analyzed for successful completion and error situations are indicated by coded halt-displays and optionally selected printouts of pertinent control information.

The controls necessary to run ESCR are simplified so that even relatively inexperienced personnel can use it. However, expandability features provide program controls limited only by the software experience of the user and memory restrictions.

2. APPLICABLE DOCUMENTS

2.1. Computer and channel product descriptions

P.D. P-10044, Rev. D	9200 System
P.D. P-10055, Rev. B	9300 System
S.U. 00039	9000 Series I/O Interface, 8-bit Compatible

2.2 Readers

C.S. 1955	Card Readers, Internal
P.D. P-10072	600 CPM Reader and Control Unit
P.D. P-10078	1000 CPM Reader and Control Unit
P.D. P-10050	1001 Card Controller

2.3 Printers

P.D. P-20077	Bar Printer Family
P.D. P-10066	900/1100 LPM Drum Printer and Control Unit

2.4 Punches

P.D. P-20066	Standard 75 CPM Punch
P.D. P-10056	9000 Series Row Punch

2.5 Tapes

P.D. P-10052	9000 Series 6-C Subsystem
P.D. P-10054	U12/U16 Magnetic Tape Subsystem
P.D. P-20041	Uniservo 6-C
P.D. P-20040	Uniservo 8-C
P.D. P-20102	Uniservo 12
P.D. P-20103	Uniservo 16

2.6 Discs

P.D. P-10068	8410 Disc File Control Unit
P.D. P-20112	8410 Disc File
P.D. P-10076	5024 Disc File Control Unit
P.D. P-21108	5024 Disc File

2.7	Punch Paper Tape	
	P.D. P-22128	9000 Series Punch Paper Tape Subsystem
2.8	Data Communications	
	S 90037	DCS 1,4 Data Communications Subsystems
	SA 00798	DCS 1,4 Data Communications Subsystems
2.9	Other Devices	
	P.D. P-10073	ICCU

3. ROUTINE ESCR

3.1 Purpose

3.1.1 On-line input/output subsystem checkout requires software facilities to handle the following general hardware considerations.

A. Both Multiplexer and Selector Channel controls and data transfer rates.

B. "Test-facility" features, such as

- device simulation
- monitor mode
- data-turn-around test mode

C. Control Unit and/or Device optional hardware features providing selection of

- recording methods
- recording densities
- odd and even parity generation
- data conversion
- data translation

D. A convenient method for data generation.

E. Any arbitrary command selection and handling of associated termination status indications.

F. An optional command selection sequence to be used when errors are detected and a "repositioning" of the device is necessary.

G. No interrupt, one interrupt, two interrupt and "unsolicited" interrupt situations.

H. Command chaining.

3.1.2 The purpose of this control routine is to easily and conveniently provide these requirements. To simplify the operating procedures, as much automatic control was built into the routine as possible.

3.2 Equipment Configuration Requirements

The primary equipment requirements for Routine ESCR are

A. Central Processor, 9200 or 9300 16K, or larger, memory size, for normal operation, 8K requires address changes outlined in Operating Instructions, Section 3.4.

B. General Purpose Channel, Feature SH03602

or

Dual Input-Output Channel, Feature F1104

C. 80 Column Card Reader or 1001 Card Controller for loading the object deck.

D. High Speed Printer (Internal), Feature F0864
132 print positions, 63 characters
- printouts are optionally selected, so this device is required only when printing is desired.

Table III lists the input-output devices which can be operated by using Routine ESCR.

3.3 Description

3.3.1 Routine ESCR executes in consecutive order, three arbitrarily selected commands, referred to hereafter as C1, C2, and C3. These commands will be issued to three optionally selected device addresses, DA1, DA2, and DA3, such that C1 will be issued to DA1, C2 to DA2, and C3 to DA3. The three device addresses may refer to the same or different devices, in any combination, using either or both types of channels.

3.3.1.2 If using a dual channel configuration, the routine will automatically detect selector channel device addresses and load the corresponding selector channel address word (CAW) into locations 78 and $79_{(16)}$. This address points to the location of the selector channel command word (CCW). If multiplexing, the address of the first byte of the four-byte buffer control word for the corresponding DA must be indicated.

Refer to Appendix I for detailed descriptions of selector and multiplexer channel control words; device commands, status, and sense indicators; and general operating procedures for controlling input-output devices.

3.3.2 The selector channel control words (CCW1, CCW2, CCW3) and the multiplexer channel buffer control words (BCW1, BCW2, BCW3) can be arbitrarily set by the operator and must conform to the requirements dictated by the associated command, the device, and the memory configuration limits of the CPU, if data transfers are involved.

3.3.3 All error and control locations in memory are preset to specific values before the execution of each of the three commands, to facilitate manual verification of changes. These preset locations are itemized in Table I.

3.3.4 After each of the three commands are initially executed, a halt-display of the following format occurs:

$$00CX_{(16)}$$

where X = 1, 2, or 3 — the command number.

These halts are bypassed on all successive execution cycles of the three commands, and their basic purpose is to allow manual verification of termination indications. A secondary purpose of the halt and reset-halt instructions is to provide memory space for "operator key-ins". These key-ins could transfer to "operator subroutines" which would perform specific testing functions or data comparison functions on the data associated with the command just terminated.

3.3.5 All errors on command execution detected by ESCR result in a halt-display (of the address of the halt-display instruction itself), followed by two branch (47) instructions. The first branch goes to the "general recovery" procedure set up for that halt and the second is designated as a "recovery switch".

3.3.5.1 The address displayed by the error halt instruction performs two functions.

1. If continuous operation is desired, all error-halts are easily ignored by one general procedure. Set up in the address switches of the control console the error-displayed address, display the contents of this address to verify the A9 operation code of the halt instruction*, and manually alter the A9 to a 47 (no-operation, branch conditional instruction). No reference to write-ups or codedits is necessary.

2. On initial use of the routine, this displayed address should be used to reference the codedit location of the halt-display instruction or Table II, where explanations for the halts are given and recovery procedures indicated. Since error checking is generalized, the number of error stops is small. Thus, error address displays and meanings usually are readily memorized.

3.3.5.2 The error halt instruction plus the two branch conditional instructions following it may be used for "operator-keyed" recovery procedures or tests. If this is not done, the first branch conditional transfers control to a subroutine which resets the program controls necessary to proceed with the execution of

*This display step may be omitted.

the next command. If the error halt is bypassed, continuous operation is accomplished and scoping facilitated.

3.3.5.3 In addition to the normal halt-displays on error, a printout of pertinent information concerning the command-in-error termination status can be obtained by selecting an option bit.

It is also possible to optionally select printouts of this same information after successful completion of each command. Selection of both options results in printing the same relevant information for both successful completion and error termination of the commands. Thus, a "hard copy" of the command sequence and termination indications is available. (Refer to Operating Instructions, Section 3.4).

The formats for printouts are given in Section 3.5 along with explanations of the heading abbreviations and fields.

3.3.6 The detection of unsuccessful completion of a command is made by the following comparisons:

3.3.6.1 CASE 1 XIOF issued in Processor Mode with command termination signaled by interrupts.

Type 1 One interrupt per command accepted (CC = 00)

The contents of locations 40, 41, 42, $43_{(16)}$ are compared to the following hexadecimal values:

CPU INTERRUPT INDICATORS*				Channel Type	Device Type
40	41	42	43		
FF	FF	00/04	DA	Multiplexer	Internal
FF	FF	0C	DA	Multiplexer	External
DA	SS	0C	DA	Selector	External

Type 2 Two interrupts per command accepted (CC = 00)

The contents of locations 40, 41, 42, $43_{(16)}$ are compared after each interrupt, as indicated,

	CPU INTERRUPT INDICATORS*				Channel Type	Device Type
	40	41	42	43		
Interrupt 1	FF DA	FF SS	08 08	DA DA	Multiplexer Selector	External External
Interrupt 2	FF DA	FF SS	04 04	DA DA	Multiplexer Selector	External External

3.3.6.2 CASE 2 XIOF issued in Input/Output Mode with command termination determined by TIO instructions.

Type 1 One end-status presentation per command accepted (CC = 00)

The contents of the end-status stored by the TIO instruction is compared to the expected value, as indicated.

TAG DS CONTENTS OF LOCATION 08CA*	CHANNEL TYPE	DEVICE TYPE
00/04	Multiplexer	Internal
0C	Multiplexer	External
0C	Selector	External

Type 2 Two end status presentations per command accepted (CC = 00)

The contents of the end-status stored by each of two TIO instructions is compared, as indicated,

	TAG DS CONTENTS OF LOCATION 08CA*	TAG DS + 1 CONTENTS OF LOCATION 08CB*	CHANNEL TYPE	DEVICE TYPE
TIO1	08	--	Multiplexer	External
	08	--	Selector	External
TIO2	--	04	Multiplexer	External
	--	04	Selector	External

*Indicator definitions (hexadecimal)

FF = Preset value
00/04 = Successful completion status for internal devices only
0C = CHANNEL END, DEVICE END
Successful completion status for external devices
DA = Device Address
SS = Selector Channel Error Indicators. Compared to 00 for no error.
08 = CHANNEL END status
04 = DEVICE END status

3.3.7 Routine ESCR expects interrupts for each XIOF issued in processor mode that has set the respective condition code to an acceptance state (CC = 00). On interrupt, end-status is tested for the ATTENTION bit, if successful completion status has not been received. If set, an unsolicited interrupt printout occurs and any outstanding expected interrupts associated with the XIOF will still be anticipated.

3.3.7.1 All other interrupts for which the processor mode PSCW indicates an address range outside of that defined by the XIOF and its associated BC instructions are considered as unsolicited, regardless of the contents of the stored status. This includes the so-called "soft-interrupt" which is generated on certain devices to indicate that a command has been issued to the device when it is in a "stop" state. The command itself is rejected and an associated interrupt generated which serves the purpose of alerting the processor to the rejection. The command-rejection-halt must be followed by hitting START to allow the "soft-interrupt" to be accepted by the processor.

3.3.7.2 When operating in I-O mode, in order to accept status presented by devices not addressed in the TIO instructions (considered unsolicited status), the following procedures may be taken. When the command-rejection-halt occurs because the Control Unit is in a pending status state, set the recovery branch conditional to address 0666 where an LPSC sets up the I-O PSCW to analyze interrupts and gives control to processor mode for one instruction time.

3.3.7.3 If loading ESCR from cards, unsolicited interrupts are handled if they occur after the first instruction (LPSC) within ESCR is executed. If initial loading from tape, the interrupt generated by the operator-initial-loading is indicated as unsolicited, as well as all interrupts which are not routine initiated by the acceptance of an XIOF instruction (CC = 00).

3.3.8 The number of end-status indications expected by ESCR is determined by testing a mask constant against the command byte of the accepted XIOF just issued. If this test mask sets CC = 11, two end-status states will be anticipated, CHANNEL END alone, followed by DEVICE END alone. Otherwise, one end-status indication of CHANNEL END and DEVICE END is expected.

3.3.8.1 Three mask constants must be set (TM1, TM2, and TM3) such that TM1 relates to C1, TM2 to C2, and TM3 to C3. If C1, C2, and C3 are all associated with the same device, the 3 test masks should have identical values based upon the Control Unit logic which makes this same determination in the hardware. For most purposes, mask bytes set to 07 are sufficient for designating "control-type" commands resulting in two end-status conditions.

3.3.9 Two data generators are optionally selectable in ESCR. The first is based on the need for a relatively small amount of data and is selected by designating bit 6 of the option selection byte. Eight bytes of data pattern are set in location 0230 →0237, tagged DATA, at the initial-load halt-display of 00EE. Before any commands are executed, this 8-byte data pattern is repeated for a total of 256 bytes in each of the 3 normal data areas beginning at locations 1000, 2000, and $3000_{(16)}$. These data patterns will remain set until GENERAL CLEAR, START reinitializes the routine. If the patterns in DATA are changed after GENERAL CLEAR, the new data pattern will be generated on START.

3.3.9.1 The second data pattern generator is based upon the need for large amounts of data generation and has a basic 16-byte repeat cycle. Bits 6 and 4 of the option selection byte must be set to designate this data generator. A 16-byte data pattern is entered in locations 0230 →23F. This pattern is repeated for a total of 8192 bytes beginning in data area 1000 before C1 is executed and will not be regenerated until GENERAL CLEAR, START reinitializes the beginning of the routine, at which time it can be altered.

3.4 Operating Instructions

3.4.1 Load Procedures

3.4.1.1 Card Deck Versions

Initial-load routine by placing the standard 4-card loaders in front of the object deck and following normal card load procedures. Halt-display 00EE indicates successful loading of deck.

3.4.1.2 Tape Version

Three identical blocks (Blocks 2, 3, and 4) containing $4000_{(10)}$ bytes of object coded data for ESCR are written (800 BPI density, NRZI recording mode) after the first locator block (Block 1) or each 9300 Test Program Master Tape. If Block 2 cannot be loaded without error, loading of Blocks 3 or 4 can be attempted or a second tape servo utilized.

Step 0: Set Control Unit to On-Line State
Step 1: Mount Master Tape.
Step 2: Set Device Address of servo in data entry switches.
Step 3: Set LOAD switch to ON position.
Step 4: GENERAL CLEAR, START loads Block 1. Repeat Step 4 once. Block 2 is loaded.
Step 5: Successful load is verified by no light bit for the UNIT CHECK indicator in the Control Unit.
Step 6: If Block 2 is loaded without error, Reset Load switch. START* or GENERAL CLEAR, START results in 00EE display.

*If GENERAL CLEAR does not clear the pending initial load interrupt, an unsolicited printout will give the pertinent information associated with this interrupt.

Step 7: If block loaded is in error, repeat Steps 3 and 4 until the 3rd or 4th block is read successfully.
Step 8: If Step 7 fails, repeat Steps 1→7 on a different servo.

3.4.1.3 Operation

The uses of this routine are determined by the operator and it is to be considered a software tool. To encompass the wide variety of hardware and software experience of users, a set of examples follow which illustrate basic operational characteristics. Following the examples, is a detailed and comprehensive reference for users extending the routine to their own particular needs, the Option Parameter Chart.

3.4.1.3.1 This program executes three XIOF instructions and handles all contingencies of status and sense. It provides a printout of each one at its successful or unsuccessful completions. The operators basic responsibility is to supply Device Address, Commands to be executed, addresses and contents of Buffer Control Words and/or Channel Command Words.

3.4.1.3.2 The data needed for these key-ins (locations 01FC → 0204 and 0206 → 023F) is found in Sections 2. to 18. Location 0205 is the Option Selection Byte. The contents of locations 0206 - 0211 is Buffer Control Word information which is dependent on the associated I-O command. If the machine used does not have all the devices called out in the examples, substitutions should be made to accommodate the configuration, as long as rules for that device are followed.

3.4.1.3.3 A quick method to try the routine would be to run one device only. All three Commands must be used since the program executes all three. In the case of one device only, the same starting BCW address should be keyed-in to 01FC, 01FD, 01FE; the same Device Address into 01FF, 0200, 0201; the three commands in 0202, 0203, 0204 and the associated BCW's in 0206 → 9, 020A → D, 020E → 0211. Each of the three XIOF's will be executed; therefore, it is very important that some valid command to some valid device be designated.

EXAMPLE OPERATION 1

Purpose: Read a card thru on-line reader, print it on bar printer and reproduce card on serial punch.

Loc.	Data	Reason
01FC	44	Starting address of reader BCW (BCW for $XIOF_1$)
01FD	50	Starting address of bar printer BCW (BCW for $XIOF_2$)
01FE	4C	Starting address of serial punch BCW (BCW for $XIOF_3$)
01FF	01	Readers device address (DA for $XIOF_1$)
0200	03	Printers device address (DA for $XIOF_2$)
0201	02	Punch device address (DA for $XIOF_3$)
0202	02	Reader Command (Read) (XF for $XIOF_1$)
0203	01	Printer Command (Print & Space) (XF for $XIOF_2$)
0204	01	Punch Command (Punch) (XF for $XIOF_3$)
OPTION BYTE		
0205	44	Stop before XIOF (Bit 1) Print on error (Bit 5) (See OPT for other options possible)
0206-9	00500080	BCW data for reader (load 80-col. into mem. beginning at loc. 80).
020A-D	01XXXXXX	BCW data for printer (mem. loc. 50 is the only one loadable -- for line space).
020E-11	00500080	BCW data for punch (punch 80-col. from mem. loc. 0080).

These are the only data insertions necessary for the above purpose.

3.4.1.3.3 continued . . .

EXAMPLE: OPERATION 2

Purpose: Read card from reader put it on tape and punch it on row punch

LOC.	DATA	REASON
01FC	44	Starting address of reader BCW (BCW for $XIOF_1$)
01FD	60	Starting Address of channel 8's tape BCW (BCW for $XIOF_2$)
01FE	58	Starting address of row punch (BCW for $XIOF_3$)
01FF	01	Reader device address (DA for $XIOF_1$)
0200	C0	Channel 8 device address tape 0 (DA for $XIOF_2$)
0201	06	Row punch device address (DA for $XIOF_3$)
0202	02	Reader command (Read -- XF for $XIOF_1$)
0203	01	Tape command (Write -- XF for $XIOF_2$)
0204	11	Row punch command (punch & feed - XF for $XIOF_3$)
	OPTION BYTE	
0205	C5	Set NRZI (Bit 0) - Sense & Monitor bits edited & printed out Stop before XIOF (Bit 1) Print on error (Bit 5) Print on successful term (Bit 7) (see OPT for other options possible).
0206-9	05001000	BCW data for reader (load 80-col. into memory beginning at loc. 1000)
020A-D	80501000	BCW data for tape (write 80 bytes on tape from memory beginning at loc. 1000).
020E-11	80501000	BCW data for punch (punch 80 bytes on row punch from memory beginning at loc. 1000)

Special changes needed for this example because of peripheral mode of operation.

0339	03	A valid mode set command for VIC tape which is needed to execute bit 0 of 0205 option byte (see sec. 11 for further definition)
01FB	11	Change test mask formate to accommodate row punches interrupt seq. where channel end and device end are returned separate (see for further definition)

3.4.2 Option Selection and Parameter Entry

After OOEE display, set option selection byte and control parameters as indicated. START initializes routine. (Superscripts refer to notes at end of this chart).

ADDRESS*	TAG REFERENCE	PRESET CONTENTS*	DESCRIPTION
01F9(1)	TM1	07	Test Mask constant for determining if CX, if accepted, will initiate 2 end-status presentations. X = 1
01FA(1)	TM2	07	Same as TM1 except X = 2.
01FB(1)	TM3	07	Same as TM1 except X = 3.
01FC(2,3,4,5)	MBC1**	70	Address of first byte of the 4-byte buffer control word area for CX, DAX. X = 1.
01FD(2,3,4,5)	MBC2**	70	Same as MBC1 except X = 2.
01FE(2,3,4,5)	MBC3**	70	Same as MBC1 except X = 3.
01FF	DA00**	E0	Device Address for C1
0200	DA01**	E0	Device Address for C2
0201	DA02**	E0	Device Address for C3
0202	C123	01	Command 1 (C1) - Standard Write
0203	C123	27	Command 2 (C2) - Standard Control (Backspace block)
0204	C123	02	Command 3 (C3) - Standard read
0205 Bit 0(6,7)	OPT	00 0 1	Option Selection Byte Do not execute MODE SET 2 command at routine initialization before C1 Execute this MODE SET 2 command.
Bit 1		0 1	Do not HALT-DISPLAY before XIOF execution. HALT-DISPLAY before XIOF execution to enable cycling.
Bit 2		0 1	Execute XIOF in Processor Mode. Do not stack status. Execute XIOF in Input/Output Mode. Stack status.
Bit 3(6,7)		0 1	Do not execute MODE SET 1 command at routine initialization before C1. Execute MODE SET 1 command.
Bit 4(8)		0 1	Execute C1, C2, and C3 sequentially. Execute C1. Execute C2 & C3 only on error.
Bit 5		0 1	Do not print on error. Print on error.
Bit 6		0 1	Do not utilize 256 byte data generator Utilize 256 byte data generator if bit 4 is not set. Utilize 8192 data generator if bit 4 is set.

3.4.2 continued . . .

ADDRESS*	TAG REFERENCE	PRESET CONTENTS*	DESCRIPTION
continued ... 0205 Bit 7	OPT	 0 1	 Do not print on successful XIOF termination. Print on successful termination.
0206→0209(9)	BCW1***	80401000	Buffer Control Word (BCW1) for C1,DA1
020A→020D(9,10)	BCW2***	80402000	Buffer Control Word (BCW2) for C2,DA2
020E→0211(9,10)	BCW3***	00403000	Buffer Control Word (BCW3) for C3,DA3
0212,0213(1,11,12)	CCW1+	021A	Selector Channel Address Word pointer for C1
0214,0215(1,11,12)	CCW2+	0222	Selector Channel Address Word pointer for C2
0216,0217(1,11,12)	CCW3+	022A	Selector Channel Address Word pointer for C3
0218→021F(1,12,13)	CW1+	01001000 10000040	Selector Channel Command Word for C1, DA1
0220→0227(1,10,12,13)	CW2+	01002000 10000040	Selector Channel Command Word for C2, DA2
0228→022F(1,10,12)	CW3+	01003000 10000040	Selector Channel Command Word for C3 DA3
0230→023F(14,15)	DATA	--	Area for Data Patterns

*Value is designated in hexadecimal
**Reference - Table III - Section 2
***Reference - Section 3
+Reference - Section 4

Note 1) This parameter is not set if the associated device address is for an internal device. The constant 07 is sufficient for most control units for external devices. However, exceptions exist and this constant should be changed accordingly. Refer to Section 1, paragraph 3.3.8.

Note 2) These bytes are not set for Selector Channel devices.

Note 3) For communications devices utilizing buffer control word areas beginning in address 0200, this byte should refer to the least significant byte of the first address of the 4-byte BCW area. In addition, the MVC instruction byte for the corresponding command should be changed as follows:

COMMAND	MVC ADDRESS	INITIAL VALUE	CHANGE TO
C1	04C4	00	02
C2	04D4	00	02
C3	04E4	00	02

3.4.2 continued . . .

Note 4) For internal devices where only 1 byte of the BCW is actually used, only this byte of the BCW need be designated in BCWX (X=1,2, or 3) but all 4 bytes will be moved to the area designated by this address.

Note 5) For a single Multiplexer Channel system, BCW addresses 0078 and 007C require location 03A5 to be changed from 7A to 80. On dual channel configurations, these addresses are restricted to selector devices only and are preset by ESCR to the Selector Channel Address Word.

Note 6) MODE SET 1 command byte is located in 030F preset to 4B.
MODE SET 2 command byte is located in 0339 preset to CB.
For tape control units 0858 and 5017, command byte 4B sets device simulation mode and command byte CB sets 800 BPI, 9-track, NRZI (5017 only) recording mode. If printing options in location 0205 and tapes are designated by DAX (X=1,2, or 3) being set to C0→CF, E0→EF or 60→6F SENSE and MONITOR SENSE modes are automatically handled to obtain sense data. MODE SET 1 will also be reissued to set Device Simulation Mode which gets reset by the MONITOR MODE operations. For external devices other than tapes, only a SENSE command is issued to obtain sense data. For internal devices, no sense data is available.

Note 7) MODE SET 1 and MODE SET 2 command bytes are issued only to DA1. Therefore, devices requiring such control are required to be associated with DA1, C1.

Note 8) C2 and C3 are usually Control and Recovery type commands. They should be previously tested to assure execution without error, for the basic purpose of this option is to have an "error-free" output.

Note 9) To be set only if device is on Multiplexor channel.

Note 10) On 8K memory configurations byte counts and data address locations should be altered to reflect the smaller memory.

Note 11) These addresses can be altered to designate operator-keyed chained command lists. These lists, however, should have the last command agree with the first command in the list with respect to the number of end-status indicators to be expected on completion of the chain.

Note 12) These parameters are set only if the corresponding designates a Selector channel device.

Note 13) These commands can designate chaining if the restrictions of Note 11) are met.

Note 14) The 16 data bytes are preset to

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
FF	A9	FF	81	D7	A9	FF	A9	44	12	44	3A	6C	12	44	12

Note 15) To be considered only if data generation is designated in 0205, Refer to Section 1, paragraph 3.3.9.

3.5 Printed Messages

3.5.1 Two types of printed information are produced by ESCR. The first type is associated with unsolicited interrupts and will print one line of the following information:

UNSOLICITED INTERRUPT ** AABBCCDD EE
AA = Selector Channel Device Address
= 00, if unsolicited MX interrupt occurred before routine presets this location
= FF, if unsolicited MX interrupt occurred after routine presets this value
BB = Selector Channel Error Status
= 00
= FF same as AA
CC = Device Status
DD = Device Address
EE = 00
= FF same as AA

This printout is not optionally selectable in location 0205. However, it maybe bypassed by altering 062A, B from a 45C0 to 4700.

3.5.2 The second type of printout is associated with initial and termination control indicators for the XIOF currently accepted and is optionally selected by setting bits 6 and/or 7 of 0205. Bit 6 maybe set at any time to control error printouts. Bit 7 should be set at initial load to print on successful completion of the XIOF.

3.5.2.1 This printout consists of one header line printout, a data line for each XIOF (in error or successfully completed, depending on the options selected). If the device is a tape unit (refer to Section 1, Paragraph 3.4.2 Note 6), one or more lines of additional information will decode in 4 alpha-numeric-character-notations each bit set in the SENSE and MONITOR SENSE bytes (refer to Section 11, Page 11-2 for Control Unit 0858 or Section 16, Page16-3 for Control Unit 5017).

3.5.2.2 Since the 6-C Control Unit is permanently assigned to channels 8 and 9, the SENSE byte decode associated with this unit requires NRZI (bit 0 of 0205) recording to be indicated and the MODE SET 2 command designated as a valid command for this unit (CB is invalid for 6-C). Refer to Section 11, Paragraph 1.18.

3.5.2.2 If a 5017 Control Unit is put on channels 8 and 9, the proper SENSE byte bit decode is obtained by altering 07C9 from 80 to F0.

3.5.3 The header and data fields for the second printout are indicated below.

3.5.3 continued . . .

FIELD NO.	DATA TYPE	HEADER DESIGNATION - DATA CONTENTS	DESCRIPTION
1		ESCR	Routine name
	1		Data field is blank
2		DENSITY	Mode Set 2 indicator
	1	PHASE	Bit 0 of 0205 = 0
	2	NRZI CB	Bit 0 of 0205 = 1 - 5017 CU
	3	NRZI △△	Bit 0 of 0205 = 1 - 0858 CU
3		INSTRUCTION	XIOF instruction
	1	AABBCCDD	AA = XIOF operation code (A4) BB = Device Address CC = 00 DD = Command Code
4		40414243	Processor Mode Interrupt Indicators
	1	AABBCCAA	AA = Device Address - SEL CHAN = 00 - if not yet preset, - MX CHAN = FF - if preset, MX CHAN BB = 00 - normal SEL CHAN indication = 80 - error SEL CHAN indicator = 40 - length error SEL CHAN indicator = 00 - if not yet preset - MX CHAN = FF - if preset, MX CHAN CC = Stored Status for Device
5		DS	Status Stored by TIO
	1	AA	AA = 00 if not yet preset & I-O set = FF if preset & PM set = XX - termination status
6		78797A7B7C7D7E7F	SEL CHAN termination CAW
	1	AAAABBBBCCCCDDDD	AAAA = Address pointer to CAW BBBB = Termination Data Address CCCC = Termination Byte Count DDDD = Error indicators
	2	-	This area is blank, if multiplexing

3.5.3 continued . . .

FIELD NO.	DATA TYPE	HEADER DESIGNATION - DATA CONTENTS	DESCRIPTION
7		COMDBADRFLAGBCNT	SEL CHAN CCW
	1	AAOOBBBBCCOODDDD	AA = Command Byte OO = Always zero BBBB = Initial Data Address CC = Chaining, Termination, Length, Indicators DDDD = Initial Byte Count
	2		This area is blank, if multiplexing.
8		TERM-BCW	MX CHAN termination Buffer Control Word
	1	ABBBCCCC	A = Data direction, Data Address Increment/Decrement, and termination Indicators. Also MS bit of byte count. BBB = Termination Byte Count CCCC = Termination Data Address
	2	--	This area is blank if selecting.
9		INIT-BCW	MX CHAN initial Buffer Control Word
	1	ABBBCCCC	Indicators are identical to Field 8 above except they reflect initial rather than termination values.
	2	--	This area is blank if selecting.
10		S0S1S2S3S4	Five Sense Byte Indicators
	1	AABBCCDDEE	AA = Sense Byte 1, hexadecimal BB = Sense Byte 2, hexadecimal CC = Sense Byte 3, hexadecimal DD = Sense Byte 4, hexadecimal EE = Sense Byte 5, hexadecimal
	2	FFFFFFFFFF	This field is preset to FF if no Sense data is available
11		M0M1M2M3M4	Five monitor Sense Byte Indicators
	1	AABBCCDDEE	AA = Monitor Sense Byte 1, hexadecimal BB = Monitor Sense Byte 2, hexadecimal CC = Monitor Sense Byte 3, hexadecimal DD = Monitor Sense Byte 4, hexadecimal EE = Monitor Sense Byte 5, hexadecimal
	2	AAFFFFFFFF	AA = Device Address base FF = Preset value - no Monitor Sense Data
12		SIM	MODE SET 1 indicator
	1	N	Bit 3 of 0205 = 0
	2	Y	Bit 3 of 0205 = 1

3.6 Program Stops

3.6.1 All program stops are listed in Table II of Section 2. They are divided into 2 types: TYPE 1 - coded halt displays; TYPE II - address-display-halts

3.6.2 Explanations and Recovery Procedures for each stop are given.

TABLE I

PRESET LOCATIONS

Reference Tag	Hexadecimal Location	Preset Hexadecimal Value	Description
NSNS	→ 0268 026C	5 bytes set to FF	Five bytes of normal sense information.
MSNS	→ 026D 0271	5 bytes set to FF	Five bytes of monitor sense information.
STATUS	→ 0040 0043	4 bytes set to FF	Channel and device status-address interrupt locations.
DS	08CA	1 byte set to FF	Device status set by a TIO instruction.
	→ 007A 007F	6 bytes set to FF	Selector channel command termination control words.
	→ 001D 001F	3 bytes	Multiplexer channel error termination status indicators and device address.

TABLE II

TYPE I — HALT-DISPLAY STOPS

ROUTINE CONTROL TYPE, CODED-HALT-DISPLAYS

Hexadecimal Display	Explanation	Recovery Procedure
00EE	Successful-initial-load	Key-in option selections and parameters. START initializes routine.
00CX X=1,2, or 3	Command X (CX) has been completed. This halt normally occurs once, after initial execution of CX.	Manually check termination indicators for CX. START initializes next command.
3ESS(1)	Printer error. SS = printer status	Correct error. START resumes printing. (NOTE: ESCR should be run without printer-loop-control to avoid 3E06 error stop.)
3AAA(1)	Printer abnormal.	Check and correct abnormal condition. START resumes printing.
3EEE(1)	Printing has been attempted resulting in an unrecoverable indication (2).	I. START reissues 3EEE halt-display. II. Set location 093B from FØ (16) to 00(16). START reissues print command.

(1) These displays occur only if printing has been attempted. The first character of the display indicates the printer channel number, 3.

(2) This stop is considered unrecoverable by the routine for normal operation. Recovery must be operator controlled as indicated.

TABLE II

TYPE II - HALT-DISPLAY STOPS

ADDRESS-DISPLAY TYPE

HEXADECIMAL DISPLAY	EXPLANATION	RECOVERY PROCEDURE
053A(3)	Bit 2 of Option-Selection-Byte (location 0205) is set to 1. (Halt-before-command-execution option).	I. 1) Manually verify initial command control indicators 2) START initiates the command II. 1) Same as I. 1) 2) Set INST switch to STEP position 3) START staticizes the XIOF about to be executed in locations 6,7,8,9(4) 4) Set CYCLE switch to cycle through the execution of this XIOF 5) Set any desired Test Mode Switches during cycling 6) On completion of the XIOF, reset INST switch to RUN position. START resumes routine.
0546(3)	XIOF instruction(4) has been rejected with Condition Code set to 01, 10, or 11.	I. 1) Verify Condition Code setting in location 0000 if in PM(5) or location 0010 if in IO(6) 2) Correct rejection condition 3) Set the address of the branch instruction following this halt to transfer control to an "operator-keyed" recovery or 4) If the rejected command is to be reissued (i.e., device was BUSY), set this address to 053E. 5) START executes the recovery step in 3) or 4)

TABLE II
TYPE II - HALT-DISPLAY STOPS
ADDRESS-DISPLAY TYPE
continued . . .

HEXADECIMAL DISPLAY	EXPLANATION	RECOVERY PROCEDURE
058C	XIOF instruction(4,5) has been accepted and end-status interrupt indicates other than OC-CHANNEL END, DEVICE END.	General Recovery 1, 2, or 3.
05AA	XIOF instruction(4,5) has been accepted and end-status for a two interrupt command does not indicate CHANNEL END on the first interrupt.	General Recovery 1, 2, or 3.
05CC	Same as 05AA except this time the second interrupt is expected containing DEVICE END.	General Recovery 1, 2, or 3.
0644	An unanticipated transfer to I-O mode has occurred. An UNSOLICITED INTERRUPT printout indicates pertinent information.	General Recovery 4.
066A	Previous LPSC did not work. A pending interrupt should have given control to location 0556 tagged INT.	I. 1) Manually verify interrupt indications. 2) START attempts to set PM. II. 1) Same as I. 1) 2) Set following branch instruction to go to operator keyed recovery. 3) START transfers control to this coding. III. General Recovery 3
068A	Previous LPSC did not transfer control to location 0390 in I-O. Probably CPU malfunction. No automatic routine recovery is provided.	I. 1) Analyze appropriate error indicators. 2) Set recovery branch instruction to transfer control to operator keyed recovery III. General Recovery 3

TABLE II
TYPE II - HALT-DISPLAY STOPS
ADDRESS-DISPLAY TYPE

continued . . .

HEXADECIMAL DISPLAY	EXPLANATION	RECOVERY PROCEDURE
069E	XIOF instruction(4,6) has been accepted. End-status stored in 08CA by a TIO indicates 00 instead of non-zero end-status.	General Recovery 1, 2, or 3
06BA	XIOF instruction(4,6) has been accepted. End-status stored in 08CA by a TIO does not indicate 0C-CHANNEL END, DEVICE END.	General Recovery 1, 2, or 3
06D2	Same as 06BA above except CHANNEL END alone end-status is expected for first of two end-status indications.	General Recovery 1, 2, or 3
06EA	XIOF instruction(4,6) has been accepted and CHANNEL END status cleared. A subsequent TIO has not set CC = 01.	General Recovery 1, 2, or 3
0702	Same as 06BA above except DEVICE END alone end-status is expected for second of 2 status indications (stored in 08CB).	General Recovery 1, 2, or 3
0722	Same as 06BA except TIO has not stored 00 or 04 for end-status on an internal device.	General Recovery 1, 2, or 3
072E	An interrupt has set I-O and control given to INT coding. The address in 2, 3 of PM PSCW should not contain a value less than 0502 Probable CPU malfunction.	General Recovery 3

NOTE 3 - Displays address of A9 halt-display instruction. This halt maybe removed by changing the A9 of the displayed address to a 47.

NOTE 4 - The XIOF instruction for C1, C2, or C3 is located in locations 053E, 053F, 0540, 0541.

NOTE 5 - PM - Processor Mode is set.

NOTE 6 - IO - Input/Output Mode is set.

TABLE II
TYPE II - HALT-DISPLAY STOPS
ADDRESS-DISPLAY TYPE

continued . . .

General Recovery 1

Step 1. Check appropriate command termination indicators.
Status 40, 41, 42, 43
TIO Stored Status 08CA, 08CB
Buffer Control Words
Condition Code Settings
Selector Channel Address Words 78 → 7F
MX Channel Error 1D, 1E 1F

Step 2. Set Print-on-error option - Bit 5 of 0205, if printing is desired and this option was not selected on initialization.

Step 3. START will print pertinent information, if printing options are set, and resume execution of next command.

General Recovery 2

Step 1. Record displayed-address

Step 2. Same as Step 1 of General Recovery 1.

Step 3. Alter the two branch conditional instructions following this halt instruction to transfer control to an operator-keyed recovery or test, or appropriate recovery coding in ESCR.

Step 4. START initializes Step 3.

General Recovery 3

Step 1. Same as Step 1 of General Recovery 1.

Step 2. Reset options and parameters, if required or desired.

Step 3. GENERAL CLEAR, START reinitializes C1.

General Recovery 4

Step 1. Same as Step 1 of General Recovery 1.

Step 2. START returns control to place at which routine was interrupted.

TABLE III

9200/9300 DEVICE ADDRESS ASSIGNMENTS

Purpose:

To define the device addresses and associated control word areas for all sub-systems that can be connected to all 9200/9300 systems.

Explanation:

There are two "BCW" areas in memory allocated for device addressing at present. The first "BCW" area is limited to eleven (11) usable sub-channels, 5_{16} through F_{16}. The maximum number of sub-systems allowed on the channel is eight (8). A single sub-system control unit can accommodate up to eight (8) devices in a shared format. Both shared and non-shared control units can use sub-channels 5_{16} through F_{16}. The second "BCW" area, sub-channels 40_{16} through $4F_{16}$, are limited to non-shared type device addressing only.

The following tabulation gives the complete device addressing assignments. The first six addresses (5_{16} through 10_{16}) have been in effect for some time. Some of the unused sub-channels are in reserve for sub-systems that are to be included in the product line in the near future.

Device	Hexadecimal Sub-channel Number	Hexadecimal Device Addresses	Hexadecimal Buffer Control Word Area
Reader (Internal)	01	01	44
Read/Punch (Internal)	02	02	48
Punch (Internal)	02	02	4C
Printer (Internal)	03	03	50
8410 Disc	05	A8	54
Row Punch	06	06	58
1001 Card Controller	07	B8	5C
VI-C Tape #1	08	CØ-7	60
VI-C Tape #2	09	C8-F	64
ICCU 418/1108-9300	0A	ØA	68
0768 Printer	0B	ØB	6C
Punch Paper Tape	0C	E0	70
DCS-4 Output #1	40	40	200
DCS-4 Input #1	41	41	204
DCS-4 Output #2	42	42	208
DCS-4 Input #2	43	43	20C
DCS-4 Output #3	44	44	210
DCS-4 Input #3	45	45	214
DCS-4 Output #4	46	46	218
DCS-4 Input #4	47	47	21C
DCS-1 Output #1	48	48	220
DCS-1 Input #1	49	49	224
DCS-1 Output #2	4A	4A	228
DCS-1 Input #2	4B	4B	22C

TABLE III

92/9300 DEVICE ADDRESS ASSIGNMENTS (cont)

Device	Hexadecimal Sub-channel Number	Hexadecimal Device Addresses	Hexadecimal Buffer Control Word Area
*U12/U16	0C Multiplexer	E0 → E7	70
	0D Multiplexer	E8 → EF	74
	-- Selector	60 → 67	78 → 7F
	-- Selector	68 → 6F	78 → 7F
*5024 Disc	-- Selector	30 → 37	78 → 7F
*600 CPM Reader	08 Multiplexor (non-shared)	08	60 → 63

*Arbitrary assignments for 9300 peripheral test-evaluation of 9400 devices.

1. INPUT/OUTPUT CONTROL

1.1 Various sets of memory locations are assigned to each input/output unit. Each set consists of four memory bytes, called a buffer control word, which is used for storing data storage addresses, character counts, and other details of each input/output function, if using the Multiplex Channel. Channel Command and and Channel Address Words (Sect. 4) are used if Selecting.

Input/output control requires the following software steps:

(1) Load the proper Control Word with information required by the control unit, provided the unit is not busy.

(2) Issue an input/output instruction which specifies the device address and the function to be performed.

(3) Check the condition code setting to determine if the instruction was accepted.

(4) Test the status of the device when the operation is completed (normally indicated by the generation of an interrupt) to determine if the operation was successful.

1.2 Processing continues during the execution of all I/O instructions. If the H bit is set to one, all interrupts for devices on a Multiplex Channel are inhibited. The Test I/O instruction should then be used to determine device status. An I/O interrupt can only be made at the end of a program instruction execution in the Processor Program State Control. At the end of each instruction execution, the peripheral interrupt request line is examined. If an interrupt request is present, interrupt is granted, control is shifted to the I/O Program State Control, and the device address and device status are stored in fixed locations in memory.

1.3 A Control Word should not be altered during the execution of an input/output operation on the peripheral device to which it is assigned. To do so can cause unpredictable results.

2. INPUT/OUTPUT INSTRUCTIONS, XIOF and TIO

2.1 The input/output instructions use the SI format. The I_2 portion specifies the I/O device. The least significant byte of the XIOF instruction specifies the command. If bit 16 of the instruction is a 1, the function is indexed before being executed.

		Operand 2		Address of Operand 1	
XIOF Op Code		Immediate Operand I_2	Base Reg. B_1	Displacement D_1	
0 A4	7	8 Device Address	15 16 19	20 Command	31

NOTES:

1. The control word associated with the device specified must have been loaded with the proper control information for this device.

2. If the instruction is executed with interrupt inhibited, the status or device address is never stored automatically. The procedure to be followed is the same as if I/O operations are done in I/O mode. In particular, the interrupt pending bit is set when the I/O operation is completed.

3. The function specification in the OP1 portion of the instruction defines the type of operation to be initiated.

4. Some devices require additional information in the Control Words.

5. Bit 27 (the H bit) is reserved to inhibit the generation of all interrupt requests when the operation ends. In this case, the interrupt pending bit will be set at the completion of the instruction.

6. Condition Codes:

   0 - Function accepted
   2 - Function rejected
   3 - Function rejected - invalid device number

   If a function is rejected, a TIO instruction causes the status to be stored to indicate a reason for the rejection.

7. A control unit is busy from the time it accepts an I/O instruction until either an Interrupt Request is granted or until it is reset by the TIO instruction.

8. When an interrupt request is granted, the indicators of the device are reset, and the status of the device is stored in memory location 42. The device address is stored in memory location 43.

2.2 Test I/O Status tests the status of the I/O unit specified by the device address in the I_2 field.

	Operand 2		Address of Operand 1
TIO Op Code	Immediate Operand I_2	Base Reg.	Displacement D_1
0 A5 7	8 Device Address 15	16 19	20 Address For Status 31

NOTES:

1. The status of the addressed unit is stored at the address specified by OP1 regardless of the ultimate condition code setting.

2. This instruction clears the device status storage in the device if it is not busy. If the device is busy, status is not reset.

3. The interrupt request is part of the device status and is cleared by this instruction.

4. Condition Codes:

   0 - Zero Status - device available
   1 - Valid Status - interrupt was pending; device now available
   2 - Busy Status - device not available (also set if the reader, punch or printer is offline)
   3 - Zero Status - invalid device number

3. Multiplexer Channel Control

3.1 Multiplexer Channel Instructions

When Execute or Test I/O instructions are issued to devices other than the basic peripherals (Device Address 1, 2, or 3), the channel will attempt to execute the initial selection sequence or I/O command. The channel will reject the command if the addressed device is offline or does not exist. This will produce condition code 3.

3.2 Multiplexer Channel Status Byte

At the time of initial selection during an Execute I/O or Test I/O instruction and also at the end of I/O operations, peripheral units present a status byte with the following format:

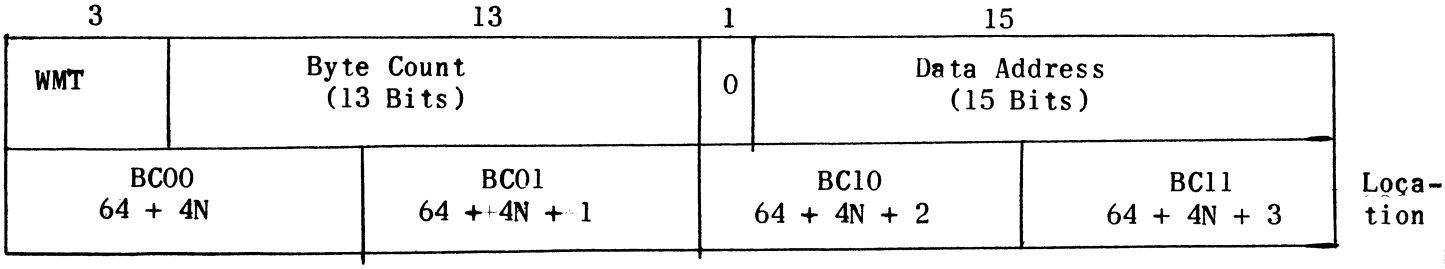
Bit 0 - Attention
    1 - Status modifier
    2 - Control Unit end
    3 - Busy
    4 - Channel end
    5 - Device end
    6 - Unit check
    7 - Exception

The status byte is stored in a program specified location by a Test I/O instruction. When the channel is allowed to interrupt the program, the status byte is stored in location 66_{10}.

3.2 Multiplexer Channel Buffer Control Word

3.2.1 When a subchannel is used, the proper BCW must be loaded with the correct initial conditions before issuing an Execute I/O order to any subchannel. Each subchannel requires a four-byte buffer control word in the main memory. The buffer control words contain initial data counts and working data counts, data addresses, and control bits. Eleven buffer control words have been reserved for the multiplexer channel (memory locations $84\text{-}127_{10}$). It may also use buffer control words allotted to basic I/O units if they are not present.

3.2.2 When a control unit initiates a sequence in order to request or present data or to present a status byte, the control unit presents a device address along with appropriate control signals. This address is placed in the multiplexer channel's device address register where it is used to determine the location of the proper buffer control word. The action taken by the channel depends upon the contents of this location. The normal BCW format follows:



Basic Format: WM ≠ 11

W = Data Direction Bit

W = 1 for write (output) or "buffered" control operations
W = 0 for read (input) operations

M = Addressing Mode Bit

M = 0 for forward addressing sequence
T = Termination Bit

If T = 1, no data will be transferred, the BCW will not be modified by the channel and the Terminate response will be given to data request.

The channel will set T = 1 after the transfer of a byte of data causes the byte count to go to zero. The channel will not reset the T bit to 0.

Byte Count: This field is decremented by the channel whenever a byte of data is transferred. An initial count of zero gives a block length of 8192 bytes if T = 0.

A control unit may terminate an operation before the count becomes zero. Upon termination, this field indicates the difference, if any, between the initial byte count and the number of bytes actually transferred.

Data Address: This field is fetched by the channel and used as the address for the current byte of data. The address is modified in the BCW under control of the M bit in preparation for the next byte. Upon termination this field indicates where the next byte would have gone to or come from had the operation continued.

The W and M bits and the I-O command initiated via the subchannel must agree.

3.2.3 Line Terminal Format WM = 11

11TB	STATUS 4 5 6 7	K	0	DATA ADDRESS 8 Bits Fixed	7 Bits Variable
BC00		BC01		BC10	BC11

T - (Terminate Bit) - if T = 1 no data will be transferred, the Data Address will not be modified, the Channel will give the Terminate response to Data Requests. The Channel will set T = 1 when "Wrap-around error" occurs (see B Bit below). The channel will not erase a T bit.

B - (Buffer End Bit) - When the address modification generates a carry from the 2^5 bit position of the Data Address (when the address is modified to an integral multiple of 64_{10}) the Channel sets the B bit to one and generates a LT Summary Interrupt Request. The B bit alerts the program that a 64-byte buffer segment has ended. The program is expected to remove the B bit when that buffer segment is again ready for use by the Channel. If the Channel finds a B bit remaining in the BCW when the End of Buffer Segment occurs again the Channel sets the T bit to one so that the data will not be overlaid. This is the "Wrap-around error" situation. The channel will not erase a B bit.

DATA ADDRESS - This field contains the address of the next data byte to be transferred. The address modification in the LT format is always A + 1→A (Mod 128). This sequence, with the B bit, gives the effect of alternating the use of two adjacent 64-byte buffer areas.

STATUS FIELD - When a device operating in the LT mode initiates a sequence to present status, bits 4-7 of the Status Byte are merged (OR function) into this field. If the CPU allows the Interrupt, the entire status byte is also placed in the DEVICE STATUS area (see memory map) and the LT Summary Interrupt Request is reset. If the Interrupt is not allowed the LT Summary Interrupt Request is set.

3.2.3 continued . . .

K Field - Address trap - If a device operating in the LT mode attempts to present status and bits 4 and 5 in the STATUS field of the BCW were previously both zero, the 8 least significant bits of the Data Address are transferred to the K field. If either bit 4 or bit 5 in the BCW was previously a one the transfer does not occur.

SELECTOR CHANNEL CONTROL

1. Selector Channel Instructions

The Selector Channel Execute or Test I/O instructions are identical to those of the Multiplex Channel and are described in Section 2. The primary difference between the two channels lies in the way control information is set up. See paragraph 3.

2. Selector Channel Status Byte

This byte is identical to that specified in Section 2, Paragraph 3.2. However, locations 40 → 43 contain vital information relative to the Command issued.

Loc 40: Device Address. Modified in Processor or I/O Mode only by Selector Channel.

Loc. 41: EL000000

E = any error, except L.
L = Incorrect length error.

Modified only by the Selector Channel.

Loc. 42: Device Status. Modified by MX. or Sel. Channel.

Loc. 43: Device Address. Modified by MX. or Sel. Channel.

Locations 41. 42, & 43 - modified only in Processor Mode.

3. Selector Channel Address Word

Locations 78 and 79 must contain the address +2 of the first byte of the 8-byte Channel Command Word and must be loaded before the XIOF is issued. On termination of the Command, locations 78 → 7F contain information related to the data transfers and error information.

MEMORY RESERVED FOR THE SELECTOR CHANNEL CAW

78	79	7A	7B	7C	7D	7E	7F
Command Add. Word		Ending Add + 1		Ending Byte Count		Error and Interface	

Loc. 78 & 79: Initially, address of 1st CCW+2.
At termination, last CCW address executed +8.

Loc. 7A & 7B: Initially, not used.
At termination, last data address +1.

Loc. 7C & 7D: Initially, not used.
At termination, number of bytes left to transfer.

Loc. 7E:
Bit 0 Interface Error
Bit 1 Address Error
Bit 2 Parity Error
Bit 3 Address Out
Bit 4 Select Out
Bit 5 Operational In
Bit 6 Address In
Bit 7 Command Out

Loc. 7F:
Bit 0 Status In
Bit 1 Service Out
Bit 2 Service In
Bit 3 Request In
Bit 4 Suppress Out
Bit 5 Select In
Bit 6 Terminate F/F
Bit 7 SJBO (always 1)

4. Channel Command Word

4.1 Channel Command Words must also be set up prior to XIOF execution. Commands may be chained, as indicated, and can reside in any appropriate 8 bytes of memory. If chained, they can be related by the Transfer In Channel (TIC) Command, which simply replaces the address field of the Address Pointer of the Channel Address Word with the Address of the TIC CCW.

4.2 The format of the Channel Command Word follows:

CHANNEL COMMAND WORD (CCW)

00	01	02	03	04	05	06	07
0 7	8 15	16 23	24 31	32 39	40 47	48 55	56 63
Command		Starting Address		Flags		*Byte Count	

Command:			
	Test	P	XXXX0000
	Sense	P	DDDD0100
	Write	P	DDDDDD01
	Read	P	DDDDDD10
	Read Backward	P	DDDD1100
	Control	P	DDDDDD11
	TIC	P	XXXX1000

P = Odd Parity Bit X = Ignored by CU's D = Detail Bits

Starting Address: Address of first byte

Flags: P OCTS0000

C = Command Chaining
T = Terminate
S = Suppress Incorrect Length Error

Byte Count: Exact number of bytes to be transferred
* (All zeros = maximum byte count = 64K)

NOTE: The CCW is never modified by the Selector Channel.

Card Reader Control

1.1 The card reader reads a card in either translate mode or in image mode.

1.2 Card Reader Instructions

The Execute I/O instruction for the card reader has the following format:

OP CODE A4	DA 00000001	B_1	00000	000H	0X10
0 7	8 15	16 19	20 23	24 27	28 31

where: X = 0 Read Translate Mode
X = 1 Read Image Mode
H = 1 Inhibit all interrupts

These two combinations of bits, in the direct $B_1 - D_1$ field or the indexed $B_1 - D_1$, are the only permissible combinations of reader XIOF instructions. Any other combination may cause an error.

1.3 Card Reader Buffer Control Word

The buffer control word for the card reader contains the following data:

HTS	COL.	BASE ADDRESS
0 7	8 15	16 23 | 24 31

where: HTS = Hardware temporary storage reserved for the reader. This byte should not be loaded by the program.
Col.. = The number of columns to be read. This must always be 80. This count will be decremented to zero to signal the end of the operation.

Base Address = The address of the most significant halfword (even numbered address) of the card read area in memory. Upon completion of the operation, this address will be one greater than the address of the last byte into which information was read.

2. Card Reader Status Bytes

2.1 The status byte contains information pertaining to the result of the last issued order or the next to last issued order. Status indications are as follows:

All zeros	No indicators set, function performed as specified.
Bit 5 set to 1	Interrupt request pending. This status bit is set only if the TIO function clears a pending interrupt before it is accepted. This status bit does not indicate an error.
Bit 1 set to 1	Misfeed, not ready, hopper empty or stacker full; these conditions are sampled only at initiation time of the XIOF instruction. If any one of these conditions exist, the XIOF instruction will be rejected. A Test I/O instruction will then store this indicator only if it follows an XIOF instruction which was rejected because of one of these conditions.
Bit 0 set to 1	Stacker jam, control parity or photocell check; instruction may or may not have been accepted and card may have been fed.

2.1.1 The error conditions are divided into Type I and Type II. Type I errors set bit 0 of the status register as soon as they occur. Type I errors indicate that the data read into memory in this card read may not be correct and should not be used by the program. Type II error indications are stored in intermediate error storage when they occur. When the next XIOF is executed, they will set bit 1 of the status register. Type II errors are delayed until a subsequent XIOF because the data read into memory during the card cycle in which they occurred is correct and can be used by the program.

2.1.2 All error conditions must be cleared manually. All error indications except Control Parity Error can be reset by depressing the Reader CLEAR switch. The Control Parity Error indication can be cleared by depressing the processor CLEAR switch. In addition, the Hopper Empty-Stacker Full (HESF) indicator can be reset by depressing the OFF-LN switch. The HESF indicator can be cleared in this way without error even if the processor is running the issuing XIOF's to the reader.

2.1.3 Offline does not set the status register but will make the reader appear busy to the processor. Any order in progress when OFF-LN is depressed will be allowed to continue to completion.

Card Punch Control

1.1 The card punch discussed below will include the controls required for the card reader option that may be incorporated to form a card read/punch.

1.2 Card Punch Instructions

The Execute I/O instruction for the card punch and reader option has the following format:

OP CODE A4	DA 00000010	B_1	000	000H	SXRP
0 7	8 15	16 19	20 23	24 27	28 31

where: H = 1 Inhibit all Interrupts
P = 1 Punch a card
R = 1 Read a card
X = 0 Read and/or Punch a card in compressed mode
X = 1 Read and/or Punch a card in image mode
S = 1 Select Stacker. Effective only if the program stacker select feature is installed. Otherwise, this specification is ignored.

Either the R or P bit must be 1. All other bits shown as 0's must be 0's, or an error may result.

1.2.1 Feeding with no reading or punching can be done by specifying the punching of two blank columns.

The second punch stacker is an error stacker and is selected on punch errors. This stacker is program selectable. However, errors will always cause this stacker to be selected regardless of program choice. Stacker selection is given for the card in the punch wait station in the same instruction that causes it to be punched.

1.3 Card Punch Buffer Control Word

The buffer control word for the card punch contains the following data:

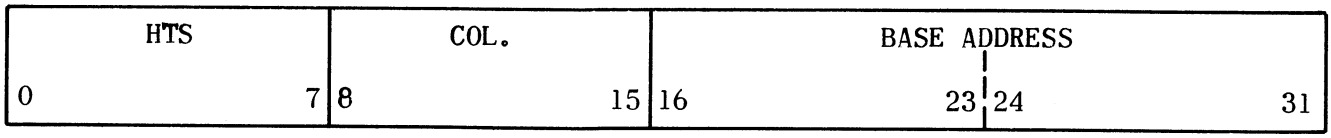
HTS	COL.	BASE ADDRESS
0 7	8 15	16 23 | 24 31

where: HTS = Hardware temporary storage reserved for the punch. This byte should not be loaded by the program.

Col. = The number of columns to be punched. This must always be an even non-zero number. At the end of a card operation this count will be decremented to zero.

Base Address = The address of the most significant halfword (even numbered address) of the card punch area in memory. Upon completion of the operation, this address will be one greater than the address of the last byte that was punched.

1.3.1 The buffer control word for the punch reader option contains the following data:



where: HTS = Hardware temporary storage reserved for the reader. This byte should not be loaded by the program.

Col. = The number of columns to be read. This must always be 80. At the end of a card operation this count will be decremented to zero.

Base Address = The address of the most significant halfword (even numbered address) of the card read area in memory. Upon completion of the operation, this address will be one greater than the address of the last byte into which information was read.

2. Card Punch Status Bytes

The status byte contains information pertaining to the result of the last issued order or to the next-to-last issued order. The status indications are as follows:

2.1 All zeros — No indicators set; function performed as specified.

2.2 Bit 6 set to 1 — Hopper empty or stacker full; when this status bit is set the last XIOF function was terminated before it was executed. To recover from this early termination, the XIOF order must be reinitiated after the condition has been corrected.

2.3 Bit 5 set to 1 — Interrupt request pending. This status bit is set only if the TIO function clears a pending interrupt before it is accepted. It does not indicate an error.

2.4	Bit 4 set to 1	Photocell check error; this is a check on the read photocells as well as possible indication of a card jam. This error indication will be registered by status bit at the end of an XIOF. The last XIOF function should be assumed in error.
2.5	Bit 3 set to 1	Data parity or control parity error; card at read station or card at punch station may be in error. An immediate interrupt occurs upon recognition of error and the XIOF is terminated. The card passing through the punch station will automatically go to the error stacker. This status bit indicates that the last XIOF instruction was probably terminated before completion.
2.6	Bit 2 set to 1	Punch check error; interrupt after card has been punched. Card being punched will automatically go to the error stacker. The status bit being set indicates that the last card punched was in error.
2.7	Bit 0 set to 1	Stacker jam, punch entry or exit check, interlocks, and any other condition that may necessitate manual intervention.

Printer Control

1.1 The printer prints first and then advances paper. To allow the maximum amount of time to prepare the next line of data and to store the data in the specified print area, interrupt is generated before the paper advance operation is completed. Thus, the functions overlap since the next XIOF instruction can be issued before the paper advance is completed for the last print instruction. If the interrupt were not generated until after the paper advance, a bar cycle would be skipped after double spacing. Printing starts when the print bar is in either the extreme left or right position. Printing then requires one complete cycle of bar movement, back and forth. An advance of as many as two lines can then be made without missing a print bar cycle.

1.2 Printer Instructions

1.2.1 Print and control are the only valid print instructions. The bar selection modifies these codes and is effective only if the Bar Printer option has been included as part of the system. Print may be given with or without paper advance. Control is used for paper feeding without printing.

The Execute I/O instruction follows:

OP CODE A4	DA 00000011	B_1	0000	BNOH	00X1
0 7	8 15	16 19	20 23	24 27	28 31

where:
- X = 0 for a Print instruction
- X = 1 for a Control instruction
- B = 0 Standard 63-Character Bar
- B = 1 Optional 48-Character Bar
- N = 1 Print Numeric if 48-Character Bar option is activated
- H = 1 Inhibit interrupt

} 9200

- B must equal N (defined below).
- N = 1 Print numeric if 16-character bar is installed
- H = 1 Inhibit interrupt
- Note: In a control XIOF, B and N are not significant

} 9300

1.2.2 On a system that has a printer with less than 132 print positions per line, data can be stored in the positions of the print image area for which there are no print hammers (locations 224 through 259, for a 96-position printer; or locations 248 through 259, for a 120-position printer). Such data is not altered by, nor does it affect, the operation of the printer.

1.3 Printer Buffer Control Word

1.3.1 The buffer control word for the printer contains the following data:

FC 0000LXXX	BA	STC	CR
0 7	8 15	16 19	20 31

where: BA = Base Address
STC = Starting Code
CR = Code Register
FC = Forms Control

CR, STC, and BA are under complete hardware control. If they are inadvertently changed by a program, a loss of printer control will probably result.

1.3.2 The forms control byte is loaded by the program once a TIO or an interrupt determines it is permissible. The forms control byte is not changed by the execution of a printer function. The four bits which designate the desired forms action follow:

L X X X

0 0 0 0 Space 0 lines
0 0 0 1 Space 1 line
0 0 1 0 Space 2 lines
1 X X X Select any of 7 paper loop channel controls by matching holes in the paper loop to the 1 bits in the X positions.

1.3.3 There are two paper loop conventions:

X X X

1 1 1 for home paper
0 0 1 for form overflow

If a hole combination is sought under paper loop control that is not punched on the tape, a runaway paper condition results.

1.4 Issue and Execute

1.4.1 "Issue" refers to the time that an XIOF is decoded by the processor and the command information is forwarded to the printer control. This is also the time at which the condition code (CC) is generated and made available to the program. "Execute" refers to the time that the printer controls respond to the command information forwarded by the processor. In some instances, "execute" may follow "issue" by a considerable period of time.

1.5 Status Register

1.5.1 The print controls contain a status register which stores the various error indications until they are transferred to memory by a TIO or by an interrupt request acceptance by the processor. When an XIOF is in progress, the setting of any bit in the status register will terminate the operation and generate an interrupt request.

1.5.1 The error conditions are divided into Type I and Type II. Type I errors set the status register directly when they occur. Type II error indications are stored in an intermediate error storage when they occur. The next time an XIOF is executed they are transferred to the status register.

1.5.2.1 Type I errors are as follows:

Bar Check
Memory Overload
Parity
Abnormal

1.5.2.2 Type II errors are as follows:

Paper Low
Forms Overflow
Paper Runaway

1.5.2.3 Bar Check occurs after an XIOF is executed, but before printing begins. Memory Overload occurs during printing.

Parity occurs after an XIOF is executed but before paper advances.

Type II errors occur during paper advance.

Abnormal can occur any time.

When an offline error occurs, the status register is not set, but the reader appears to be busy to the processor. Any order in progress when the offline (OFF-LN) switch is depressed will be allowed to continue to completion.

1.6 Interrupt Requests

1.6.1 Interrupt requests occur at the following times:

End of print before associated paper feed is started.

Immediately following an accepted paper feed order before paper advancing has begun, unless a previously initiated paper feed order is in progress. In the latter case the interrupt is delayed until the previously initiated paper feed order has been completed.

Upon abortion of an order due to detection of paper low, forms overflow, or forms runaway as a result of a preceding order.

Upon termination of an operation due to any other error condition.

2. Printer Status Bytes

The status byte (in location 66) contains information pertaining to the result of the last issued order or the next to last issued order. The status indications are as follows:

2.1	All zeros	No indicators set; function performed as specified.
2.2	Bit 7 set to 1	Paper Low* as a result of paper spacing. Until the paper condition is corrected, this indicator will occur for each XIOF. Paper low will be indicated when the bottom edge of the form is 15 1/3" ±1/3" from print line.
2.3	Bit 6 set to 1	Form overflow*. 001 sensed at paper loop station during single or double spacing. Form overflow is set even if spacing does not stop on the 001 channel punch. Passing over the punch is sufficient.
2.4	Bit 5 set to 1	Interrupt request pending. This status bit is set only if the TIO function clears a pending interrupt before it is accepted. This status bit does not indicate an error.
2.5	Bit 4 set to 1	Instruction does not agree with bar switch setting.
2.6	Bit 3 set to 1	Data parity or control parity error on last XIOF instruction. Printer stops immediately.
2.7	Bit 2 set to 1	Memory overload occurred on last XIOF instruction. Printer stops immediately. Paper has not advanced.
2.8	Bit 1 set to 1	Paper Runaway*-forms control lost. Further orders will not be accepted without operator intervention, since the printer goes abnormal.
2.9	Bit 0 set to 1	Abnormal or not ready.

*These conditions are recognized following the normal interrupt request. Therefore, the previous function will be properly completed except in the case of paper runaway where paper has been spaced improperly. If another XIOF has been accepted, it will be aborted and an interrupt will be generated. If the next XIOF is not issued until after detection of the condition, the order will be accepted, then aborted and an interrupt request will be generated. Any error that happens before paper is advanced will void paper advancing.

UNIVAC 8410 Disc File Control

1. Command Repertoire

1.1 The following command codes may be issued to the Disc File Control by the computer. Any other codes will be rejected and cause a Unit Check status to be returned to the channel.

Bit Position	XF Code	Command
	P01234567	P = Odd Parity X is ignored by the Disc File Control ABCDEF = Detail Bits.
1.2	PXX000000	Test I/O: Disc File Control sends status byte to the channel and clears the status register and Status In when the channel responds that it has accepted the status byte.
1.3	PABCDEX01	Write Commands: The following commands will be considered as write commands by the Disc File Control. Bits BCD will specify the state of the three output control lines sent to the Disc File to specify the command. If bit E = 1, a prep write is specified. If bit E = 0, a normal write is specified.
1.3.1		At the completion of the Initial Selection Sequence the unit select line, along with the output control lines and output request, will be presented to the Disc File interface to transfer the command. The Control Unit will request the first byte from the Channel Interface and when this character has been received, the Control Unit will bring up Output Request. The Output Strobe will then be brought up to allow the output data to be sampled by the Disc File. The Control Unit will request bytes of data until COMMAND OUT response is given by the channel.
1.3.2		When the Disc File has accepted a command, the Disc File busy indication will be presented to the Control Unit. This line will remain up until the completion of the command (other than Seek Track) or until the Disc File detects an error and terminates the operation. In order to sample the status of the Abnormal and Interrupt lines from the Disc File, the Unit Select and Input Request lines must be brought up. The Disc File will return an Input Acknowledge and clear the abnormal conditions when the Unit Select is dropped, if there are errors. If no errors have been detected, the Disc File will not return Input Acknowledge and the Control Unit must time out the dropping of Unit Select.

NOTE: For normal write commands, the A bit is always zero. When the A bit is a 1 a maintenance write is specified. A maintenance write responds to the channel the same as a normal write operation. However there is no command or data transfer to the

NOTE: (cont) 8410 Disc File. Unit Select, Input and Output Requests are inhibited from being sent to the 8410 Disc File. There will be no responses received from the 8410 Disc File. All responses to the channel will be generated internally by the 8410 Disc File Control.

Bit Position	XF Code	Command
1.4	P01010X01	Write and Check: The Disc File Control will receive five bytes from the channel specifying the address of a record on the Disc File. The address will have the following format:

U = Disc File unit address (from 0 to 7 in BCD).

T_M = Most significant digit of track address (from 0 to 9 in BCD).

U $T_M T_L S_M S_L$

T_L = Least significant digit of track address (from 0 to 9 in BCD).

S_M = Most significant digit of sector address (from 0 to 9 in BCD).

S_L = Least significant digit of sector address (from 0 to 9 in BCD).

	U	T_M	T_L	S_M	S_L
	oooouuuu	oootttt	ooootttt	oooossss	oooossss
Bit	01234567	01234567	01234567	01234567	01234567

1.4.1 Bit 3 of the most significant track address byte T_M will specify if a head on the movable arm or the fixed fastband head is being addressed. A zero in this bit position indicates a head on the movable arm, while a one in this bit position indicates the fixed fastband head.

1.4.2 The five bytes of address will be followed by the data that is to be written in the specified sector.* Upon completion of the data transfer, the Disc File will read the address of the track on which the specified arm is positioned and compare this against the track address specified in the buffer memory. If the address does not agree, the Disc File will position the arm to the correct track. The Disc File will return a busy signal to the Control until the completion of the write and check read. (Since the Disc File uses the same head for reading and writing, the check read requires 50 ms for additional revolution of the disc.)

*If more than six bytes (including the address), but less than the capacity of a sector are transferred to the Disc File, those locations not receiving data will be cleared to binary zeroes. If less than seven bytes are transferred, the remaining locations will contain data stored the last time the memory was loaded.

Bit Position	XF Code	Command
1.5	P00010X01	Write: This write is the same as Write and Check except that the read check is eliminated.
1.6	P0110XX01	Read: The 8410 Disc File Control will receive five bytes from the channel specifying the address of a record on the Disc File.
1.6.1		The bytes specifying the address will be transferred to the Disc File buffer. The Disc File will read the address of the track on which the specified arm is positioned and compare this against the track address specified in the buffer memory. If the address does not agree, the Disc File will position the arm to the correct track. The Disc File will return a busy signal to the control until the completion of the read. Information read will be stored in the buffer. (An Unload Buffer command must be issued to transfer data to the channel.)
1.7	P0000XX01	Seek Track: The 8410 Disc File Control will receive five bytes from the channel specifying the address of a track on the Disc File. The address format is that specified for Writes with the exception that the sector address characters have no significance. When the Unit Select to the Disc File is dropped after transfer of the address bytes, the arm will be positioned to the track specified. The busy indication from the Disc File will be returned to the Control until the address of the track the arm is presently at is read.
1.8	P0111XX01	Magnitude Search: When beginning a Search High, the Disc File Control will receive five bytes from the channel specifying the address of a record. These five bytes will be followed by the key that is being searched for.
		NOTE: All data tracks, including the fastband, can be used for this search. If a data track is used, the heads must have been positioned to the correct track by a previous Seek Track Command.
1.8.1		The key will be compared against the contents of the addressed track. When the track key area is less than the desired key followed by an equal-to or greater-than key, a comparison occurs. As a result, the address of that track and sector remains in the buffer. This address can be retrieved by issuing an Unload Buffer Command.

Bit Position	XF Code	Command
1.8.2	P0111XX01	The maximum key length that can be searched for is 160 eight-bit characters. Portions of the key may be masked by using a sentinel character to mask the beginning and ending of the key. The sentinel character is 11111111. The key search will not begin until the first non-sentinel character is recognized. The search ends when the first sentinel character occurs after the search has started.
1.9	P0011XX01	Search Equal: The 8410 Disc File Control will receive five bytes designating the record address from the channel, followed by the key that is to be searched for. All five bytes will be significant. Bit 3 of the most significant track address byte will specify a head on the movable arm, or the fixed fastband head. Sector addresses of 54 or less will select head 1. Sector addresses of 55 to 99 will select head 2.
1.9.1		When head 1 is selected. only the 55 sectors under it can be searched. Head 2 must be selected by another Search Equal Command to search the 45 sectors under it. The maximum key length that may be searched for is 160 eight-bit characters.
	NOTE:	No check is made to determine if the correct track is being searched. The head must have previously been positioned to the correct track. Intervention Required (bit position 1 of the Sense Byte) condition will occur.
1.10	P01011X01	Prep Write Normal: The Prep Write command is used to write sector addresses on a disc. One track at a time can be prepped. Before attempting this instruction, the Prep Mode Switch on the Disc File must be thrown. If this switch is not thrown the Prep Wirte will be treated as a normal write.
1.10.1		This instruction is performed the same as a Write Command. Only the address portion is significant. Addresses are of the same format as Writes.
1.10.2		When the first Prep Write command is issued, not more than 800 microseconds is permitted between successive commands. This includes Prep Write Bad Spot Commands. If sectors under head 1 are being prepped, exactly 55 valid addresses and 4 Bad Spot Commands or invalid addresses will be written. Sectors under head 2 require exactly 45 addresses and 4 Bad Spot Commands or invalid addresses to be written.

	Bit Position	XF Code	Command
1.10.3		P01011X01	In the 8410 Disc File, the Prep Write is distinguished from other write instructions by activating Input Control Line 3. in addition to the Output Control Lines being sent to the Disc File. Input Control Line 3 permits the Disc File to write the first track address after the detection of the home sprocket. This Input Control Line remains active until a command other than the prep writes or a Sense is issued from the channel. A command other than a prep write or Sense must be issued at the end of transfer of 49 or 59 addresses and bad spots. This allows the Disc File to recognize the home sprocket for the next track.
1.10.4			Before starting a Prep, it must be assured that the heads are in the home position. The Home Request switch on the Disc File must be depressed to return the heads to home. After returning home the heads are positioned to the desired track by issuing a Seek Track command. At the termination of the Seek Track the selected head will be positioned to the correct track. The Prep Write command may then be issued for that track.
		NOTE:	Any track may be selected from the home position. Once the heads have positioned to a track, the heads may only be positioned to higher numbered tracks. To position to a track with a lower address, the heads must be repositioned to the home position.
1.10.5			Instructions other than Prep Write or Seek Track may be performed when the Prep Write Switch is thrown. However, all read or write commands must be issued for the track being prepped. If the track address issued is not the same as the one the heads are positioned to, the Equipment Check Sense Bit will be set in the control.
1.11		P00011X01	Prep Write Bad Spot: This command is performed the same as a Normal Prep Write. In the 8410 Disc File Subsystem ones will be written in the Sector Address. The all-ones code masks out that sector.
1.11.1			Up to four bad spotted sectors are permitted per track. These can be used to mask non-recordable areas of a track. Once a Prep Write Bad Spot Command has been issued for a sector, there is no way to address that sector.

	Bit Position	XF Code	Command
1.11.2		P00011X01	If less than 4 sectors are bad on a track an illegal address will be written in the address area of any sectors less than the track capacity. e.g. There are 45 addressable sectors under head 2 and 4 reserved. If 3 sectors have bad spots, then the fourth sector address area will be recorded with an illegal address instead of a Bad Spot.
1.12		PAXX1XX10	Unload Buffer: The Unload Buffer command will cause the 8410 Disc File to transfer the contents of the buffer to the Disc File Control. The first five characters transferred will be the address of the record. Input Request will be generated instead of Output Request. Input Control Line 1 will also be generated.
		NOTE:	If bit A is a 1 a maintenance Unload Buffer is specified No data will be unloaded from the 8410 Disc File Subsystem buffer. Data returned will be the first 8 bit code transferred to the 8410 Disc File Control data register as a result of the last write command. This data byte will continually be sent as data until the channel signals terminate.
1.13		P0XXX0100	Sense: The Disc File Control transfers sense bytes to the computer as input data. In addition to supplying pertinent information to the program, this data can be used as maintenance aids. The sense bytes provide the detail information about the unusual conditions detected in the last operation which were initially signalled to the computer in the status byte during Status In.
1.14		P0X010000	Set Inhibit Status: This command is processed as a Test I/O Command. (If accepted, it does not generate any new status.) Status will be presented to the Channel and Inhibit Status In will be set.
1.15		P0X100000	Reset Inhibit Status: This command is processed as a Test I/O Command. (If accepted, it does not generate any new status. Status will be presented to the Channel and Inhibit Status In will be reset.
1.15.1			The condition of the Inhibit Status In can be examined in Sense Byte 1, bit position 6. When Inhibit Status is set, the Disc File Control will not initiate sequences to present status.

	Bit Position	XF Code	Command
1.17		P0X110000	Set and Reset Inhibit Status: If a command is given with both the Set and Reset Inhibit bits, the command will be treated as a Test I/O and Inhibit Status In will not be affected.

2. Status Byte

2.1 The status byte provides the overall information about status and conditions detected in the last operation. The status byte will be stored in the Status Register and will be transmitted to the channel on the BUS IN during Status In, (initiated at the end of the Initial Selection Sequence, completion of the data transfers and completion of the command). The Status Register will be cleared when the channel responds to Status In with SERVICE OUT. The following defines the significance of each status bit.

	Bit Position	Designation	Interpretation
	P	Odd Parity	Parity for status byte.
2.2	0	Attention	Not used. Bit is always 0.
2.3	1	Status Modifier	Present with busy bit to indicate Disc File Control is busy executing a previously initiated command.
2.4	2	Control Unit End	Not used. Bit is always 0.
2.5	3	Busy	Indicates that the Disc File Control cannot accept a command because one of the following conditions exists: a) Disc File Control is executing a previously initiated command. b) Disc File Control is holding pending status conditions from a previous command of the addressed unit. (Not applicable to Test I/O or Set or Reset Inhibit Status.) Busy can occur only during the Initial Selection Sequence.
2.6	4	Channel End	Indicates the completion of the data transfers between the channel and the Disc File. Channel End can only occur when Device End occurs.

	Bit Position	Designation	Interpretation
2.7	5	Device End	Indicates the completion of a command, except for Seek Track. In the case of a Seek Track, Device End indicates that motion control has begun.
2.8	6	Unit Check	Any of Bits 0, 1, 2, or 3 in Sense Byte 1 are set.
2.9	7	Unit Exception	Not Used. Bit is always 0.

3. Sense Data Byte

3.1 Sense data provide detailed information about the unusual conditions detected in the last operation and the status of the Disc File Subsystem. The Sense data will be cleared when the next command is accepted, if the command is not a Sense Command or Test I/O.

The following describes the significance of the sense data:

3.2 Sense Byte 1

	Bit Position	Designation	Interpretation
3.2.1	P	Odd Parity	Parity for Sense Byte 1.
3.2.2	0	Command Reject	Unspecified command issued to the Disc File Control. This bit is suppressed if the command byte has bad parity (Bit 2 BUS OUT Check).
3.2.3	1	Intervention Required	Indicates that the interrupt line from the Disc File is active. This indicates a no find condition on a Search command, or if present with the abnormal line, a catastrophic failure.
3.2.4	2	BUS OUT Check	Parity Error. Even parity appeared on the BUS OUT from the channel during the command or data transfer. Bit 0 (Command Reject) is suppressed when Bit 2 is indicating a parity error in the command byte.
3.2.5	3	Equipment Check	Indicates that the abnormal line from the Disc File is active.
3.2.6	4	Data Check	Not Used. Bit is always 0.
3.2.7	5	Overrun	Not Used. Bit is always 0.
3.2.8	6	Inhibit Status In	Inhibit Status In.

3.2.9

Bit Position	Designation	Interpretation
7	Input Control	Input Control Line No. 3 FF set. (Indicates control is in Prep Mode).

3.3 Sense Byte 2

This bytes provides the last command executed.

3.4 Sense Byte 3

Bit	Designation (signal)	Normal Values
0	UDATA	0
1	UACT1	1
2	UFLT (Disc File Fault)	0
3	UUSEL	0
4	$\overline{\text{UGND3}}$	0
5	UAKN	1
6	$\overline{\text{UBUSY}}$	0
7	UGND2	0

3.5 The abnormal line from the Disc File indicates the following conditions:

1. A Write Check error.
2. A Read error (on address or data) after three attempts to read.
3. Phase error on reading (check on demodulator).
4. Phase character error on reading data.
5. Motion Control Error.
6. Bit Count Check.
7. No data written, invalid track address.

3.6 The interrupt line from the Disc File indicates a No Find error during a Search command.

Both the abnormal and interrupt active at the same time indicate the following conditions:

1. More than a single unit selected.
2. Disc File power off.

9000 Series Row Punch Subsystem

1. COMMAND REPERTOIRE

1.1 The following command codes may be issued to the punch control by the Processor. Any other codes will be rejected and will return a Device check status to the Processor.

	Bit Position	Command P01234567	Description
			P = Odd Parity Bit X = Ignored by control unit ABCDEF = Detail Bits
1.2	PXX000000 or PXX110000	Test IO:	The punch control presents a status byte to the channel. Service Out from the channel clears the status.
1.3	PAXXXXF10	Unload Buffer:	(Read): Data read from the previous card to the buffer is transferred to the Channel. At the completion of the data transfer, the punch control presents Status to the channel. F = 0 Read in the compress mode. F = 1 Read in the image mode. A* = 1 Unload Punch Buffer A = 0 Unload Read Buffer *This function is provided for Buffer Memory and Translator test.
1.4	PAXCDEX11	Control	This code is used for non-data transfer operations in the punch control unit. E = 1 Feed a card. The cards are advanced one station. D = 1 Feed and punch a card. C = 1 Feed a card and select stacker. The card which was punched on the previous punch order will be placed in the select stacker. A* = 1 Post-punch read to punch buffer. A = 0 Normal operation *Maintenance Feature.

COMMAND REPERTOIRE (continued)

	Bit Position	Command P01234567	Description
1.4			If the R/P Feature is present, the pre-read station is transferred to the buffer when a card is fed.
1.5	PAXCDEF01	Load Buffer	(Write): Information is transferred from the channel to the punch buffer. At the completion of the data transfer, the control unit presents Status to the channel. If the channel issues an early termination of the data transfers, the control unit will fill the remaining locations of the buffer with binary zeros. The load buffer function will normally be accompanied by the feed and punch Detail Bits. F = 0 Write in the compress mode. F = 1 Write in the image mode. Bits C thru E are specified under Control. A* =1 Load Read Buffer A =0 Load Punch Buffer *Buffer test. (A and D should not both be ones).
1.6	PXXXX0100	Sense:	The punch control transfers two sense bytes to the computer as input data. The first sense byte generally sypplies details about any unusual conditions that occurred during the last operation. The channel can issue an early termination if the transfer of all sense bytes is not desired.
1.6.1			Prior to transmitting the sense data to the channel, the control unit will test the punch. The results of the test will modify the sense by setting additional flip-flops. The status will not be modified and no sense bits will be reset.
1.7	PXX010000	Set Inhibit Status:	This command is processed as a Test I-O Function. Status will be presented to the channel and Inhibit Status In will be set.
1.8	PXX100000	Reset Inhibit Status:	This command is processed as a Test I-O Function. Status will be presented to the channel and Inhibit Status In will be reset.

2. STATUS BYTE:

2.1 The status byte supplies information pertaining to conditions of the last operation. The status byte will be presented to the channel at the following times:

1. The end of the Initial Selection Sequence.
2. The completion of data transfers on the load or unload buffer commands.
3. The completion of card motion cycles.

The status register will be cleared when the channel responds to "Status In" with Service Out. The following list defines use of the bits in the Status Byte.

	Bit Position	Designation	Interpretation
2.2	P	Odd Parity	Parity for Status Byte.
2.3	0	Attention	Not used. Bit always 0.
2.4	1	Status Modifier	Signaled with the busy bit to indicate that the control unit is busy either performing a previously initiated function or holding pending status on a unit other than the addressed unit
2.5	2	Control Unit End	Not Used. Bit always 0.
2.6	3	Busy	Indicates that the control unit cannot accept a command because of one of the following reasons: (a) Control is executing a previously initiated operation. (b) Control is holding pending status conditions from a previous operation of a unit other than the addressed unit. (c) Control is holding pending status conditions from the addressed unit.
2.6.1			Conditions (a) and (b) also present the status modifier bit. Busy can occur only during the Initial Selection Sequence. Busy will not be set if the command issued in (c) is a test I-O.
2.7	4	Channel End	If the selected device is the row punch, channel end indicates the completion of the data transfers between the buffer and the channel, or the acceptance of a control function. If Channel End is "stacked," the Control Unit will disconnect and try to present the status when the priority allows.

STATUS BYTE (continued)

	Bit Position	Designation	Interpretation
2.7.1	4 (cont)		Following is a list of conditions which will present channel end: (1) Completion of data transfers during a punch order. (2) Acceptance of a control immediate function. (3) In an unload buffer function, channel end is presented with device end when the buffer to channel transfers are completed. (4) Channel End will be presented if a data parity error causes an early termination.
2.8	5	Device End	Indicates the completion of a function initiated by the channel. In the Row Punch, Device End is presented in the following cases: (1) At the completion of a punch command. (2) At the completion of a control immediate function. (3) Presented with Channel End when the data transfers during an unload buffer function are completed. (4) Presented when an error occurs which will not allow the completion of the punch command.
2.9	6	Unit Check	One or more bits were set in Sense Byte 1 (bits 0 thru 5 or 7) when sampled by Channel End or Device End.
2.9.1			A parity error in the Function Byte, an Invalid Function or a Unit Abnormal when tested in the Initial Selection Sequence has been detected. In these cases, the Unit Check is sent to the channel during the Initial Selection Sequence
2.9.2			The punch was found to be non-ready when tested during Initial Selection. The function will be rejected and no end status will be generated. The normal sense bits will be set to indicate the type of error that occurred.
2.10	7	Unit Exception	If the selected device is the Row Punch, Unit Exception indicates a hole count error on the previous punch cycle. Unit Exception will be presented to the channel with Device End.

3. SENSE DATA BYTES:

3.1 Sense data provides information about unusual conditions that occurred during the last operation. The sense information will be cleared when the next function is accepted, if the function is not a sense function or a test I-O. The status of various flip-flops in the control unit are transferred to these bytes. These bytes are to be used for error recovery routines or for maintenance functions in conjunction with failure finding routines.

3.2 Sense Byte 1:

	Bit Position	Designation	Interpretation
3.2.1	P	Odd Parity	Parity bit for Sense Byte 1.
3.2.2	0	Command Reject	An unspecified command was issued by the channel. This bit is supressed if bad parity is detected during transfer of the function code. Neither Channel End nor Device End is set in the status. The Invalid Command codes for the Row Punch are: PXXXX1X00 and PXX000X11
3.2.3	1	Intervention Required	A punch error, other than Hole Count, was detected during the previous operation. The fault may be empty hopper, stacker full, A jam, B jam, non-ready, stacker jam or full chip box. All errors with the exception of Hole Count require manual intervention.
3.2.4	2	Bus Out Check	Parity error on the function or data transfer to the control unit. If the control unit is not holding pending status, a parity error during the function transfer causes immediate termination and the suppression of Invalid Function. Neither Device End nor Channel End will be set in the Status Byte. If the control unit is holding pending status, a parity error during the function transfer will be ignored. The sequence will be handled as if the control unit was holding pending status and the function byte had good parity. Parity error during data transfer causes immediate termination. Channel End will be presented. Error status will be presented with Device End.
3.2.5	3	Card Jam	A card transport error has occurred. A jam in the pre-punch station will light the A jam indicator on the punch control panel. A jam in the post-punch station will light the B jam indicator on the punch control panel.

Sense Data Byte 1 (continued)

	Bit Position	Designation	Interpretation
3.2.6	4	Data Check	Not used. Bit is always 0.
3.2.7	5	Data Late	The buffer has not been loaded prior to the initiation of punching.
3.2.8	6	Inhibit Status In	Inhibit Status In is set.
3.2.9	7	Non-Repeat Abnormal	Hopper Empty, Chips, Stacker Full, Stacker Jam.

3.3 Sense Data Byte 2:

	Bit Position	Designation	Interpretation
3.3.1	P	Odd Parity	Parity Bit for Sense Byte 2.
3.3.2	0	Not used	
3.3.3	1	Not used	
3.3.4	2 Punch 3 Hole 4 Counter	HCRPA HCRPB HCRPC	Prior to the initiation of a card cycle, these bits contain the weighted hole count of the card in the Punch Station.
3.3.5	5 Post- Read 6 Hole 7 Counter	HCR2A HCR2B HCR2C	Prior to the initiation of a card cycle, these bits contain the weighted hole count of the card in the Post-Read Station.

9000 SERIES 1001 CONTROL

1. COMMAND REPERTOIRE

1.1 The following command codes may be issued to the 1001 Control by the computer. Any other codes will be rejected and cause a Unit Check status (without Device End and Channel End) to be returned to the channel.

	XF Code	Function
Bit Position	P01234567	P = Odd Parity X is ignored by the 1001 Control. ABCDEF = Detail Bits

1.2 PXX000000 or PXX110000 TEST I-O: 1001 Control sends a status byte to the channel and clears the Status Register and Status In when the channel responds that it has accepted the status byte.

1.3 PABCDEF10 READ: (Read Device Buffer)
Sequence for Card Controller:

The 1001 Control is in an input request mode and the Card Controller is on an output step.

Detail Bits Specified:

A = 0 Normal Operation
A = 1 Maintenance Mode. Command is executed in 1001 Control without initiating any action in the Card Controller or other device.

BCD: Not used with the Card Controller. When Feature F0822-01 is included Bits BCD are presented to the systems slave interface on the 3 input control lines.

E = 0 Inhibit sending check character to the addressed unit.

E = 1 Send check character to the Card Controller.

F = 1 6-bit mode.
F = 0 Compress mode

COMMAND REPERTOIRE (continued)

		XF Code	Command
1.4		PABCDEX01	WRITE: (Transfer to Device Buffer) Sequence for Card Controller: The 1001 Control is in an output request mode and the Card Controller is on an input step. The 6 least significant bits of each 8-bit byte from the channel are transferred to the Card Controller. Detail Bits Specified: Same as READ Command except "BCD" are presented to the systems slave interface in the 3 output control lines. Also, Detail Bit F is not used.
	Bit Position	XF Code P01234567	Command
1.5		PAXXX0100	SENSE: The 1001 Control transfers the Sense byte to the computer as input data. In addition to supplying pertinentinformation to the program, this data can be used as maintenance aids. The sense byte provides detailed information about unusual conditions detected in the last operation which were initially signaled to the computer in the status byte during Status In. The Card Controller is tested for abnormal prior to transferring the Sense byte to the channel. This condition is indicated in Bit 1 of Sense Byte 1. Note that if abnormal is set during the execution of any function other than a TEST I-O or SENSE, the unit check (Bit 6) is also set in the status. Detail Bit Specified: A = 0 Normal Operation A = 1 Maintenance Mode. The operation is normal except the device test is blocked.
1.6		PXX010000	Set Inhibit Status: This command is processed as a TEST I-O Function. (If accepted, it does not generate any new status.) Status will be presented to the channel and Inhibit Status In will be reset.
1.7		PXX100000	Reset Inhibit Status: This command is processed as a TEST I-O Function. (If accepted it does not generate any new status). Status will be presented to the channel and Inhibit Status In will be reset.

COMMAND REPERTOIRE (continued)

PXX100000 (cont.)

Reset Inhibit Status (cont.)

The condition of the Inhibit Status In can be examined in Sense byte 1, bit position 6. When Inhibit Status is set, the 1001 Control will not initiate any sequences to present status. The Set Inhibit Status command should not be issued if the 1001 Control is connected on a selector channel.

2. STATUS BYTE

2.1 The Status byte provides the overall information about status and conditions detected in the last operation. The Status byte will be stored in the Status Register and will be transmitted to the channel on the BUS IN during the Status In. The Status In is initiated at the end of the initial selection sequence and at the completion of the data transfers. The Status Register will be cleared when the channel responds to the Status In with Service Out. The following defines the significance of each status bit.

	Bit Position	Designation	Interpretation
2.2	P	Odd Parity	Parity for Status byte.
2.3	0	Attention	Not used. Bit is always 0.
2.4	1	Status Modifier	Present with busy bit to indicate 1001 Control is busy either executing a previously initiated operation, or is holding pending status from a previous operation of a unit other than the addressed unit.
2.5	2	Control Unit End	Not used. Bit is always 0.
2.6	3	Busy	Indicates that 1001 Control cannot accept a command because one of the following conditions exists: a) 1001 Control is executing a previously initiated operation. b) 1001 Control is holding pending status conditions from a previous operation of a unit other than the addressed unit. c) 1001 Control is holding pending status conditions from a previous operation of the addressed unit. (Not applicable to TEST I-O or Set or Reset Inhibit status). Conditions a) and b) above also present Bit 1 (status modifier). Busy can occur only during the initial selection sequence.
2.7	4	Channel End	Indicates the completion of the data transfers between the channel and the Card Controller. Note early termination if abnormal is detected.
2.8	5	Device End	Same indication as Bit 4 (Channel End).
2.9	6	Unit Check	Set simultaneously with the setting of Bit 0, 1, or 2 in Sense byte 1, except if Bit 1 of the Sense byte is set when the Card Controller is tested during a sense command.
2.10	7	Unit Exception	Not used. Bit is always 0.

3. SENSE BYTE

Sense Byte

3.1 Sense data provide detailed information about the unusual conditions detected in the last operation and the status of the Card Controller (or other unit). The Sense data will be cleared when the next command is accepted, if the command is not a SENSE command or TEST I-O. The following describes the significance of the Sense Data.

3.2 Sense Byte 1

	Bit Position	Designation	Interpretation
3.2.1	P	Odd Parity	Parity for Sense Byte 1.
3.2.2	0	Command Reject	Unspecified command issued to 1001 Control. This bit is suppressed if the command byte has bad parity (bit 2 BUS OUT check). The following are invalid command codes: PXXXXX000, PXXXX1X00, PXXXXX11.
3.2.3	1	Intervention Required	Indicates Card Controller is stopped. (The Card Controller, while selected, signals abnormal on the System Slave Interface). The error or fault condition in the Card Controller may be misfeed, card jam, stacker full, or hopper empty. Manual intervention is required.
3.2.4	2	BUS OUT Check	Parity error. Even parity appeared on the BUS OUT from the channel during the command or data transfer. Bit 0, "Command Reject," is suppressed when Bit 2 is indicating a parity error in the command byte.
3.2.5	3	Run Off	Bit is 0 except in some cases following a Selective Reset or Interface Disconnect sequence.
3.2.6	4		Indicate the status of control logic flip-flops. Primarily intended to be used in conjunction with failure finding programs.
3.2.7	5		
3.2.8	6	Inhibit Status	Inhibit Status In is set.
3.2.9	7	Undefined	

Function Codes

6-C Control Unit No. 0858-XX

COMMAND	BIT POSITIONS 0	1	2	3	4	5	6	7	HEX
Set Inhibit Status	0	0	0	1	0	0	0	0	10
Reset Inhibit Status	0	0	1	0	0	0	0	0	20
Sense	0	0	0	0	0	1	0	0	04
Write	0	0	0	0	0	0	0	1	01
Read	0	0	0	0	0	0	1	0	02
Read Backward	0	0	0	0	1	1	0	0	0C
Control	0	0	C	C	C	1	1	1	
Rewind	0	0	0	0	0	1	1	1	07
Rewind with Interlock	0	0	0	0	1	1	1	1	0F
Erase	0	0	0	1	0	1	1	1	17
Write Tape Mark	0	0	0	1	1	1	1	1	1F
Backspace Block	0	0	1	0	0	1	1	1	27
Backspace File	0	0	1	0	1	1	1	1	2F
Forward Space Block	0	0	1	1	0	1	1	1	37
Forward Space File	0	0	1	1	1	1	1	1	3F
Mode Set	D	D	M	M	M	0	1	1	
No Operation	X	X	0	0	0	0	1	1	X3
Reset Fault-Finding Modes	0	0	0	0	1	0	1	1	0B
Set Device Simulation Mode	0	1	0	0	1	0	1	1	4B
Set Operation Monitor Mode	1	0	0	0	1	0	1	1	8B
Set Low Gain	0	1	0	1	1	0	1	1	5B

FOR 7 TRACK TAPE ONLY

									200	556	800
Odd Parity, Converter On	D	D	0	1	0	0	1	1	13	53	93
Even Parity, Converter Off	D	D	1	0	0	0	1	1	23	63	A3
Odd Parity, Converter Off	D	D	1	1	0	0	1	1	33	73	B3

X = Either 1 or 0
DD = tape density as follows:

00 = 200 bpi
01 = 556 bpi
10 = 800 bpi
11 = not used

Practically all other code combinations, of which there are over 200, are invalid.

UNIVAC

U6-C Subsystem Type 0858-XX

STATUS, SENSE DATA, MONITOR SENSE DATA, AND SENSE BYTE BIT-DECODE MNEMONICS*

	BIT	0	1	2	3	4	5	6	7
STATUS BYTE		ATTENTION	STATUS MODIFIER	CONTROL UNIT END	BUSY	CHANNEL END	DEVICE END	UNIT CHECK	UNIT EXCEPTION
SENSE	BYTE 0	INVALID FUNCTION *CMRJ	INTERVENTION REQUIRED *INRQ	OUTPUT BUS CHECK *BSCK	EQUIPMENT CHECK *EQCK	DATA CHECK *DACK	DATA LATE *OVRN	WORD COUNT ZERO *WDCZ	DATA CONVERTER CHECK *DCCK
	BYTE 1	NOISE *NOIS	TAPE UNIT STATUS "A" *TUSA	TAPE UNIT STATUS "B" *TUSB	SEVEN TRACK *7TRK	LOAD POINT *BOT	END OF TAPE *EOT	FILE PROTECT *TUFP	"0" *TUIC
	BYTE 2	"0" *TIE0	"0" *TIE1	"0" *TIE2	"0" *TIE3	"0" *TIE4	"0" *TIE5	"1" *TIE6	"1" *TIE7
	BYTE 3	READ VERTICAL RED.CHECK *RVRC	LONGITUDINAL REDUNDANCY CHECK *LRC	SKEW *SKEW	CYCLIC REDUNDANCY CHECK *CRC	WRITE VERTICAL RED. CHECK *WVRC	"0" *TUPH	BACKWARD *BKWD	"0" *SB37
	BYTE 4	RUNAWAY *RWAY	TAPE MOTION FAULT *TMFT	"0" *SB42	"0" *SB43	"0" *SB44	STALL *STAL	TAPE FAULT *TPFT	"0" *SB47
MONITOR SENSE	BYTE 0	PROGRAM COUNT Bit 0 *PC00	PROGRAM COUNT Bit 1 *PC01	PROGRAM COUNT Bit 2 *PC02	DENSITY Bit 0 *DEN0	DENSITY Bit I *DEN1	EVEN PARITY *EPAR	DATA CONVERTER ON *DCON	FAULT FINDING MODE ON *SIM
	BYTE 1	WRITE *WRIT	READ *READ	BACKWARD *BKWD	SPACE *SPAC	FILE *FILE	REWIND *REW	WRITE TAPEMARK *WTM	ERASE *ERAS
	BYTE 2	BACKWARD/ LOADPOINT *PRER	EARLY GAP WRITE *EGAP	TAPE MARK DETECTED *TMD	LOW GAIN *LOWG	EARLY TERMINATE *CTRM	INHIBIT STATUS IN *PSTA	CRC Bit 0 *CRC0	CRC Bit 1 *CRC1
	BYTE 3	CRC Bit 2 *CRC2	CRC Bit 3 *CRC3	CRC Bit 4 *CRC4	CRC Bit 5 *CRC5	CRC Bit 6 *CRC6	CRC Bit 7 *CRC7	CRC Bit P *CRCP	LPC Bit Ø *LRC0
	BYTE 4	LPC Bit 1 *LRC1	LPC Bit 2 *LRC2	LPC Bit 3 *LRC3	LPC Bit 4 *LRC4	LPC Bit 5 *LRC5	LPC Bit 6 *LRC6	LPC Bit 7 *LRC7	LPC Bit P *LRCP

SPECIFICATION SHEET

SPECIFICATION SYMBOL SH04479 | REVISION - | SHEET 11-2

6-C TAPE CONTROL UNIT NO. 0858-XX

1. COMMAND REPERTOIRE

1.1 The command byte is transmitted by the Channel during the Initial Selection sequence. The Control Unit checks the parity and validity before accepting the Command. Invalid Commands are code combinations not described or MODE SET Commands without the corresponding features in the Control Unit.

1.2 TEST (X X 0 0 0 0 0 0 or X X 1 1 0 0 0 0)

A TEST command initiates the sequence of presenting a status byte to the Channel at the end of Initial Selection sequence. The status may include the stored status of the addressed unit. When the status byte is accepted by the Channel, the STATUS IN pending state will be cleared and the status register will be cleared to binary zero. The TEST Command generates no new status and is completed at the end of the Initial Selection sequence.

1.3 SET INHIBIT STATUS (X X 0 1 0 0 0 0)

This Command is performed as a TEST Command. In addition, the Command sets the Inhibit Status In condition which inhibits the Control Unit from initiating the Request In sequence to present status to the Channel. Under this condition, the status will be presented to the Channel only at the end of the Initial Selection sequence. This condition remains set until reset by a System or Selective Reset, or by a RESET INHIBIT STATUS function.

1.4 RESET INHIBIT STATUS (X X 1 0 0 0 0 0)

This Command is performed as a TEST Command. In addition, the Command resets the Inhibit Status In condition.

1.5 SENSE (0 0 0 0 0 1 0 0)

The SENSE Command tests and stores the current status of the selected tape unit and then proceeds to transfer the sense bytes to the Channel. The information in the sense bytes contains the current status of the tape unit and any unusual conditions detected during the last operation. The transfer rate of the sense bytes is set to approximately the same rate as the nominal data transfer rate. The status byte presented at the completion of the SENSE Command will contain the status as the results of the SENSE operation. The status byte will contain CHANNEL END bit (bit 4) and DEVICE END bit (bit 5).

1.6 WRITE (0 0 0 0 0 0 0 1)

1.6.1 The WRITE Command moves tape on the selected unit in a forward direction. Data is fetched from the Channel and is written on tape until the Channel terminates the data transfer. The end status byte will include the UNIT EXCEPTION bit (bit 7), if a WRITE operation is performed in the end-of-tape area.

WRITE (0 0 0 0 0 0 0 1) (cont)

1.6.2 The following description of normal termination applies for WRITE, READ and READ BACKWARD operations: The end status byte, consisting of the CHANNEL END bit (bit 4) and the DEVICE END bit (bit 5) along with other status bits—if any, will be presented to the Channel when the end-of-block is detected on the Read or Check Read. The end of block is detected when the data signal from the tape has ceased for more than 800 μs.

1.7 READ (0 0 0 X 0 0 1 0)

1.7.1 The READ Command moves tape on the selected unit in a forward direction and reads a block of data from tape. The data is transferred to the Channel until the end-of-block occurs or the Channel terminates the transfer.

1.7.2 The end status byte will include the UNIT EXCEPTION bit (bit 7) if the block read is a Tape Mark Block. (The Tape Mark character will not be transferred to the Channel when detected as a single character Tape Mark block. However, if the Tape Mark code appears anywhere in the body of a multiple-character block, it will be transferred to the Channel as data.) 7-track Tape Mark is detected in both even and odd parity modes during "Read" and "Space" operations.

1.8 READ BACKWARD (0 0 0 X 1 1 0 0)

1.8.1 The READ BACKWARD Command moves tape on the selected unit in the backward direction and reads a block of data in the reverse order in which it was written on the tape. The data is transferred to the Channel until the end-of-block occurs or the Channel terminates the transfer. The READ BACKWARD operation will not be initiated if the tape is at load point on testing. In this case, the status byte presented to the Channel will contain the UNIT CHECK bit only.

1.8.2 Moving the tape backward into Load Point during the READ BACKWARD operation will cause the UNIT CHECK bit (bit 6) and the UNIT EXCEPTION bit (bit 7) to be set in status.

1.8.3 The READ BACKWARD operation in 7-track mode should not be attempted using tapes generated by other than UNISERVO VI-C, UNISERVO VIII-C, UNISERVO XII, UNISERVO XVI or other tape units which provide scatter correction of the LRC Frame.

1.8.4 The READ BACKWARD operation in 7-track data conversion mode should not be attempted with tapes having block length other than a multiple of four frames.

1.8.5 Sensing a Tape Mark is the same as in READ operations.

1.9 CONTROL (0 0 C C C 1 1 1)

CONTROL Commands involve no transfer of data. When the selected tape unit is tested and is in an operational state, the status byte consisting of the CHANNEL END bit (bit 4) only will be presented to the Channel. The end status byte will include the CONTROL UNIT END bit (bit 2) if the Control Unit was addressed or an unusual condition was detected and caused UNIT CHECK or UNIT EXCEPTION bits to be set while the Control Unit was busy independently of the Channel. The Control Unit is considered busy independently of the Channel during the interval between the TRANSMISSION of the status byte containing the CHANNEL END bit and GENERATION of the end status byte containing the DEVICE END bit. The particular control operation is specified by the modifier bits (C C C) of the function. The description of each is as follows:

1.10 REWIND (C C C = 0 0 0)

1.10.1 This command rewinds the tape on the selected unit to load point. The operation in the Control Unit terminates after the rewind has been initiated in the tape unit. The end status byte consisting of DEVICE END will be presented to the Channel.

The operation in the tape unit terminates when the tape is positioned at Load Point.

1.10.2 If the unit being rewound is addressed with a command other than a SENSE Command, the status of that Command will contain the UNIT CHECK bit (bit 6) only, to indicate the addressed tape unit is busy.

1.11 REWIND WITH INTERLOCK (C C C = 0 0 1)

This Command rewinds the tape on the selected unit to Unload point and sets the interlock condition in the tape unit. The operation in the Control Unit terminates after the rewind with interlock has been initiated in the tape unit. The end status byte consisting of the UNIT CHECK bit (bit 6) and the DEVICE END bit (bit 5) will be presented to the Channel. The normal end status byte will not include the CONTROL UNIT END bit (bit 2). The operation in the tape unit terminates when the tape is positioned at Unload Point. If a Unit under the interlock condition is addressed with a Command other than a SENSE Command, the status byte of that Command will contain the UNIT CHECK bit (bit 6) only, to indicate the addressed tape unit is unavailable. The interlock condition of the tape unit is removed only by manual intervention.

1.12 ERASE (C C C = 0 1 0)

1.12.1 This Command moves the tape on the selected unit forward and erases tape for approximately 3.5 inches. The end status byte consisting of the DEVICE END bit (bit 4) along with other bits, if any, will be presented to the Channel when the the Erase timing in the Control Unit has expired.

1.12.2 The end status byte will include the UNIT EXCEPTION bit (bit 7) if the ERASE operation is performed in the end-of-tape area. The check read is activated to

check for spurious pulses arising from any portion of the tape that is unerased.

1.13 WRITE TAPE MARK (C C C = 0 1 1)

1.13.1 This Command moves the tape on the selected unit in a forward direction and generates an interblock gap of approximately 3.5 inches by erasing, then writes a Tape Mark.

1.13.2 WRITE TAPE MARK operation for a 7-track mode overrides the parity mode setting and writes the Tape Mark with even parity.

1.13.3 The end status byte will include the UNIT EXCEPTION bit (bit 7), if the operation is performed in the end-of-tape area.

1.13.4 When the end-of-block is detected on Check Read, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the Channel.

1.14 BACKSPACE BLOCK (C C C = 1 0 0)

1.14.1 This Command moves tape on the selected unit to the next interblock gap in the backward direction. When the end-of-block is detected on Read, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the Channel.

1.14.2 The operations at or into Load Point and sensing a Tape Mark are the same as in READ BACKWARD.

1.14.3 During 7-track BACKSPACE BLOCK or BACKSPACE FILE operations, a Tape Mark may be erroneously identified on tapes generated by other than UNISERVO VI-C, UNISERVO VIII-C, UNISERVO XII, UNISERVO XVI or other tape units which provide scatter correction of LRC character. Verification of a Tape Mark is accomplished by reading forward.

1.15 BACKSPACE FILE (C C C = 1 0 1)

1.15.1 This Command moves tape on the selected unit backward to the interblock gap beyond the next Tape Mark Block. If a Tape Mark is not encountered, the tape will stop at Load Point.

1.15.2 Moving tape backward into Load Point will cause the UNIT CHECK bit (bit 6) to be included in the end status byte.

1.15.3 A BACKSPACE FILE operation will not be initiated if the tape is at Load Point on testing. The Status Byte presented to the Channel will contain the UNIT CHECK bit only.

1.15.4 Sensing the Tape Mark will not cause the UNIT EXCEPTION bit (bit 7) to be included in the end status byte.

1.15.5 When the End of Tape Mark Block is detected, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the Channel.

1.16 FORWARD SPACE BLOCK (C C C = 1 1 0)

This Command moves the tape on the selected unit forward to the next interblock gap. Sensing a Tape Mark will cause the UNIT EXCEPTION bit (bit 7) to be included in the end status byte. When the end-of-block is detected, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the Channel.

1.17 FORWARD SPACE FILE (C C C = 1 1 1)

1.17.1 This Command moves the tape on selected unit forward to the interblock gap beyond the next Tape Mark block. Sensing the Tape Mark will not cause the UNIT EXCEPTION bit (bit 7) to be included in the end status byte.

1.17.2 When the End of Tape Mark block is detected, the end status byte consisting of DEVICE END bit (bit 5) along with other bits, if any, will be presented to the Channel.

1.18 MODE SET (D D M M M 0 1 1)

1.18.1 The MODE SET Command is used to select the data transfer mode of operation. The specific mode is defined by bits 0, 1, 2, 3, and 4 of the Function. Once set, data transfer modes remain set until changed by another MODE SET Command or reset by the Channel. The reset conditions are 800 bpi and Odd Parity. If the data converter feature is installed, the reset conditions are 800 bpi, Odd Parity and Data Converter On.

1.18.2 The 7-track Mode Setting is active only with the 7-track Tape Unit and has no effect upon the 9-track operation. MODE SET Commands are completed during the Initial Selection sequence.

1.18.3 The End Status Byte consisting of the CHANNEL END bit (bit 4) and the DEVICE END bit (bit 5) will be presented to the Channel at the end of the Initial Selection sequence.

1.18.4 The MODE SET Command will not clear the sense bytes when accepted.

1.18.5 The specific MODE SET Command is defined as follows:

1.20 MODE (000)

This defines a "No Operation". No operation will be performed.

1.21 MODE (001)

This mode is used for failure-finding only. Non-diagnostic programs should not attempt to set this mode of operation.

1.22 MODE (010)

This mode defines a 7-track mode with Odd Parity, Data Converter On and a Density defined by the DD Bits.

1.23 MODE (011)

When DD = 01, this mode defines a Low Gain setting for the next "Read" or "Space" operation. The Low Gain condition will be cleared at the end of the operation following the MODE SET.

1.24 MODE (100)

This mode defines a 7-track mode with Even Parity, Data Converter Off, and a Density defined by the DD Bits.

1.25 MODE (101)

This mode is not used (invalid Command).

1.26 MODE (110)

This mode defines a 7-track mode with Odd Parity, Data converter Off, and a Density defined by the DD Bits.

1.27 MODE (111)

This mode is not used (invalid Command).

1.3 MAINTENANCE COMMANDS

1.3.1 RESET FAILURE-FINDING MODES (00001011)

This command resets the Device Simulation Mode and Operation Monitor Mode, if they were set. The control unit will return to the normal state. The System Reset, or Selective Reset, will also reset these modes.

1.3.2 SET DEVICE SIMULATION MODE (01001011)

This command activates the tape unit simulation logic. The signals to the tape unit will be blocked and simulated return signals will be generated during the execution of subsequent commands. This facilitates the checkout of the control unit without a tape unit.

1.3.3 SET DEVICE SIMULATION MODE (01001011) (cont)

1.3.3.1 For write operation, the write data received from the Channel will be processed through the write logic, then will be fed back into the read recovery logic. The Cyclic Redundancy Check (CRC) frame will be generated, but a Longitudinal Redundancy Check (LRC) frame will not be generated. However, the content of the LRC register will be the LRC frame supposed to be written on the tape.

1.3.3.2 For read operation, the content of the CRC register will be used as the simulated data. The content will be shifted end-around one place from high to low order for every frame generated. The simulated data will be generated at nominal data frequency until it receives the data terminate signal from the Channel.

1.3.3.3 The output of CRC register will be added with the R. O. pattern (111010111) in binary addition before it is gated into the read recovery logic. The CRC register will be precleared only before a write, simulated write, or read operation.

1.3.3.4 To set up desired data in the CRC register for the simulated read, a write operation should be performed beforehand. The parity of the content of the CRC register depends on the number of characters written during the previous write operation. The vertical parity checker in the read recovery can be checked with the data having a wrong parity.

1.3.3.5 If the initial content or the shifted content of the CRC register does correspond with R. O. pattern, the generated data block will have a blank frame for every ninth frame. By this, the frame dropout checker in the read recovery can be checked.

1.3.3.6 For Write Tape Mark operation, the generated Tape Mark frame will be gated into the read recovery logic.

1.3.3.7 For space, or space file operation, one frame of the generated data from the CRC register will be gated into the read recovery logic. The tape mark indications will be set if the generated data correspond with the tape mark code.

1.3.3.8 The erase operation will be executed in the normal manner.

1.3.2 SET OPERATION MONITOR MODE (10001011)

1.3.4.1 This command activates the logic which transmits the Monitor Sense bytes instead of the Sense Data bytes during the subsequent sense operation(s).

1.3.4.2 The Monitor Sense bytes (5 bytes) provide detailed information about the operational condition caused by the last operation.

2. Status Byte

2.1 The Status Byte provides the overall information about status and conditions detected in the operation completed. The Control Unit initiates the sequences to present status to the Channel at the end of the Initial Selection sequence, at the completion of unit selection of a control operation and at the completion of the operation. The status bits are reset to Binary Zero when the status presented is accepted by the Channel. The following defines the significance of Binary One in each status bit.

	Bit	Designation	Interpretation
2.2	0	Attention	Not used, always zero.
2.3	1	Status Modifier	Present with the BUSY bit to indicate Control Unit busy.
2.4	2	Control Unit End	When the Control Unit Completes a CONTROL operation that kept it busy independently of the channel, during which time it was either addressed (causing a Control Unit busy indication) or an unusual condition was detected (UNIT CHECK or UNIT EXCEPTION), CONTROL UNIT END will be presented with DEVICE END. The Control Unit is considered busy independently of the channel during the interval between the TRANSMISSION of the CHANNEL END Status Byte and the Generation of the DEVICE END status byte.
2.5	3	Busy	a) Present with STATUS MODIFIER to indicate Control Unit busy.
2.5.1			b) Present with status already stored if status pending for addressed tape unit, when the Command is other than a TEST, SET INHIBIT STATUS or RESET INHIBIT STATUS.
2.6	4	Channel End	For SENSE, WRITE, READ and READ BACKWARD Commands, CHANNEL END is presented with DEVICE END when the operation is completed at the Control Unit Level and presented on a CONTROL COMMAND, after the tape unit is tested and available. If early errors prevent tape motion, and the operation is aborted early, the CHANNEL END status bit is not sent to the channel. It is also presented at the end of initial selection with DEVICE END on MODE SET functions.
2.7	5	Device End	Indicates that the operation is complete at the Control Unit level. When errors are detected before tape motion is initiated, DEVICE END is not presented with error status. Operations that are aborted when in progress (e.g. Equipment Check) will cause DEVICE END to be sent with UNIT CHECK and CHANNEL END.
2.8	6	Unit Check	a) A bit in Sense Byte 0 has been set as a result of the current operation. If an error condition is detected before tape motion is initiated, UNIT CHECK will be presented without end status.
2.8.1			b) A READ BACKWARD, BACKSPACE BLOCK, or BACKSPACE FILE has been attempted on a tape unit with the tape positioned at load point (no end status is presented in this case).

	Bit	Designation	Interpretation
2.8.2			c) A REWIND WITH INTERLOCK has been completed at the Control Unit level, i.e. when the tape unit becomes non-ready. If the operation is initiated, DEVICE END will be presented with UNIT CHECK and CONTROL UNIT END.
2.8.3			d) The asynchronous response of busy (ready and rewinding) is indicated by presenting Unit Check without ending status.
2.9	7	Unit Exception	Indicates:
			a) A WRITE, WRITE TAPE MARK or ERASE operation is performed in the end-of-tape area.
2.9.1			b) A Tape Mark is sensed during a READ, READ BACKWARD, FORWARD SPACE BLOCK, or BACKSPACE BLOCK operation. In cases a) and b) UNIT EXCEPTION is presented with DEVICE END.
2.9.2			c) When tape is moved into Load Point by READ BACKWARD or BACKSPACE Commands, UNIT EXCEPTION is presented with CONTROL UNIT END, UNIT CHECK, and DEVICE END.

3. Sense Data Bytes

3.1 The sense data provides detailed information about unusual conditions detected in the last operation and the current status of the selected tape unit. Sense information bits that are modified with the current status of the tape unit are indicated by an asterisk(*). No additional sense information can be set as a result of executing a SENSE Command once the Command has been accepted (i.e. odd parity and valid function code).

The following describes the significance of the sense bytes.

3.2 Sense Byte 0

	Bit	Designation	Interpretation
3.2.1	0	Invalid Command	a) Set when a WRITE, WRITE TAPE MARK, or ERASE operation was attempted on a file-protected tape unit.

	Bit	Designation	Interpretation
3.2.2	0	Invalid Command (cont)	b) Set when an invalid Command is transmitted to the Control Unit (this condition will not be set if a BUS OUT check occurred on a Command transfer).
3.2.3	1	Intervention Required	Set whenever tape unit status A is inactive, i.e. a non-existent or non-ready tape unit was selected on other than a SENSE Command. (Bit 1 is not set in Sense Byte 1.)
3.2.4	2	Output Bus Check	Set whenever Even Parity appears on the BUS OUT for data or Command transfers. During WRITE operations, if this condition is set on a data transfer, the operation is terminated, and the error byte is not written on the tape. If the error occurs on the first data transfer, Word Count Zero will be set in conjunction with BUS OUT check.
3.2.5	3	Equipment Check	Set whenever an Equipment Check occurs, i.e., bits 0 or 1 or 5 of Sense byte 4 has been set.
3.2.6	4	Data Check	Set whenever a Data Check occurs, i.e., bit 0 of Sense byte 1, or bits 0, 1, 2, 3, or 4 of Sense byte 3 have been set.
3.2.7	5	Data Late	Set if service is requested on the I/O Interface but data cannot be transferred due to a late SERVICE OUT signal from the channel (not set on SENSE Command).
3.2.8	6	Word Count Zero	Set during a WRITE operation if transfer of data is prevented when the first byte of data is requested. No tape motion will occur if this condition is detected.
3.2.9	7	Data Converter Check	Set on 7-track operation only.

3.3 Sense Byte 1

	Bit	Designation	Interpretation
3.3.1	0	Noise	During WRITE or WRITE TAPE MARK operations, indicates that the GAP signal was detected sooner than was expected. False GAP can occur due to Data Dropout.

	Bit	Designation	Interpretation
3.3.1.1	0	Noise (cont)	During WRITE or WRITE TAPE MARK operations, indicates that Bit 6 of SENSE BYTE 4 is set, due to the FALSE END of block.
3.3.1.2			During READ, READ BACKWARD, FORWARD SPACE BLOCK, and BACKSPACE BLOCK operations, indicates that data was recognized after the LRC byte but not long enough after to be considered a new block. Data detected after the LRC byte set the noise bit and maintain tape motion but are not transferred. This condition can occur due to a "drop-out" of data during the block, causing a false LRC byte to be detected.
3.3.2	1*	Tape Unit Status A	Selected and Ready.
3.3.3	2*	Tape Unit Status B	Not ready, rewinding or under control of the other Control Unit.

Status A	Status B	Tape Unit Status	Bit set in Status Byte
0	0	Non-existent	UNIT CHECK
0	1	Not ready	UNIT CHECK
1	0	Ready and not busy	---
1	1	Ready and busy, i.e. rewinding.	UNIT CHECK

3.3.4	3*	Seven Track	The selected unit has a seven-track head installed.
3.3.5	4*	Load Point	The tape on the selected unit is positioned at load point.
3.3.6	5*	End of Tape	The tape on the selected unit is in the end-of-tape area.
3.3.7.	6*	File Protect	The tape on the selected unit does not have a write enable ring.
3.3.8	7		Not used - Always set to Zero.

3.4 Sense Byte 2

Bit	Designation	Interpretation
0 ↓ 7	Track in Error	Bits 6 and 7 set to 1's unconditionally upon a Data Check.

3.5 Sense Byte 3

	Bit	Designation	Interpretation
3.5.1	0	R/W VRC	a) A Vertical Redundancy Check occurred on a Data Frame or CRC Frame during a READ or READ BACKWARD operation. This indicator is not set after a Data Late indication. b) A speed check error occurred during a WRITE or WRITE TAPE MARK operation.
3.5.2	1	LRC	A Longitudinal Redundancy Check occurred during a WRITE, WRITE TAPE MARK, READ, or READ BACKWARD operation.
3.5.3	2	Skew	Excessive skew detected while read-checking recorded data on a WRITE or WRITE TAPE MARK operation.
3.5.4	3	CRC	Cyclic Redundancy Check on READ.
3.5.5	4	W/VRC	A Vertical Redundancy Check occurred on a Data Frame or CRC Frame during a WRITE or WRITE TAPE MARK operation.
3.5.6	5		Not used - Always set to Zero.
3.5.7	6*	BACKWARD	The selected Tape Unit is in BACKWARD Condition.
3.5.8	7		Not used - Always set to Zero.

3.6 Sense Byte 4

	Bit	Designation	Interpretation
3.6.1	0	Runaway Check	a) While read checking recorded data during WRITE or WRITE TAPE MARK operations, data was not detected within at least 10 ms. after writing has commenced.

Sense Byte 4 (cont)

	Bit	Designation	Interpretation
	0	Runaway Check (cont)	b) During all read-type operations, if data is not detected in at least 15 seconds.
3.6.2	1	Tape Motion Fault	a) Tape unit failed to respond to a "start" command. Tape motion may or may not have occurred. b) Tape motion stopped independently of the Control Unit during an operation requiring tape movement. (This condition will be detected if a backward operation is executed into load point.)
3.6.3	2 ↓ 4	These bits are reserved for failure-finding mode.	———
3.6.4	5	Stall	Indicates that the Control Unit is HUNG UP for more than 15 seconds.
3.6.5	6	Tape Fault	During WRITE or TAPE MARK Operation, indicates that end of block was detected sooner than expected. False End of Block can occur when the data drop in the block is longer than 800 μs.
3.6.6	7	This Bit is reserved for failure-finding mode.	———

4. MONITOR SENSE BYTES

4.1 Monitor Sense Byte 0

	Bit	Designation	Interpretation
4.1.1	0	Program Count 2^0	These three bits hold the program count when a stall condition occurs. The hold is Released when Sense byte 4, Bit 5 is cleared. Since the Monitor Sense byte 0 is transmitted to the channel during the program count of 1, the Channel normally sees $2^0 = 1$, $2^1 = 0$ and $2^2 = 0$.
4.1.2	1	Program Count 2^1	
4.1.3	2	Program Count 2^2	
4.1.4	3	Density Bit 0	Density setting in the Mode Register. The clear condition will be Bit 0 = 1 and Bit 1 = 0. If 7-track feature is not insatlled, then Bit 0 = 1 and Bit 1 = 1.
4.1.5	4	Density Bit 1	
4.1.6	5	Even Parity	Even parity mode is set and 7-track unit is selected. If 7-track feature is not installed, this bit will always be zero. This bit will be zero for the clear condition.
4.1.7	6	Data Converter On	Data converter mode is set and 7-track unit is selected.
4.1.8	7	Failure-Finding Mode	Device simulation mode is set. This bit will be zero for the clear condition.

4.2 Monitor Sense Byte 1

Monitor Sense byte 1 holds the previously accepted I/O command other than the Sense or Monitor Sense command. The sampling of the command register will be made when the tape unit is being selected. Monitor Sense byte 1 can be cleared with System Reset, but not with Selective Reset.

	Bit	Designation	Interpretation
4.2.1	0	Write	Write command.
4.2.2	1	Read	Read or Read Backward command.
4.2.3	2	Backward	Read backward, Backspace block or Backspace file command.
4.2.4	3	Space	Backspace block, Backspace file, Forward space block, or Forward space file command.
4.2.5	4	File	Backspace file or Forward space file command.
4.2.6	5	Rewind	Rewind or Rewind-with-interlock command.
4.2.7	6	Write Tape Mark	Write tape mark command.
4.2.8	7	Erase	Erase command.

4.3 Monitor Sense Byte 2

	Bit	Designation	Interpretation
4.3.1	0	Backward/Load Point	A backward command was issued at Load Point. The bit will be cleared at the beginning of the next command other than Sense or Monitor Sense.
4.3.2	1	Early Gap/Write	A gap in the record was detected earlier than expected on a write operation. A detail breakdown on Sense Byte 1, Bit 0. The bit will be cleared as was Bit 0.
4.3.3	2	Tape Mark Detected	Tape Mark was detected on a read, space, or space file operation. There is no significance on this bit for other operations.
4.3.4	3	Low Gain	Previous command was a low gain mode set command.
4.3.5	4	Data Terminate	The control unit did not receive a data terminate signal from the Channel and terminated the data transfer because of data exhaustion. This includes the case where the byte count of the channel is equal to the number of the data bytes to be transmitted. Sense and Monitor Sense commands are included. The bit will be cleared at the beginning of the next command other than Sense or Monitor Sense.
4.3.6	5	Inhibit Status In	Inhibit Status In condition is set.
4.3.7	6	CRC Bit 0	CRC register output Bit 0. The CRC register will be precleared on a write, simulated write, or read operation.
4.3.8	7	CRC Bit 1	CRC register output Bit 1.

4.4 Monitor Sense Byte 3

Bit	Designation	Interpretation
0	CRC Bit 2	CRC register output Bit 2.
1	CRC Bit 3	CRC register output Bit 3.
2	CRC Bit 4	CRC register output Bit 4.
3	CRC Bit 5	CRC register output Bit 5.
4	CRC Bit 6	CRC register output Bit 6.
5	CRC Bit 7	CRC register output Bit 7.
6	CRC Bit P	CRC register output Bit P.
7	LRC Bit 0	LRC register output Bit 0.

4.5 Monitor Sense Byte 4

Bit	Designation	Interpretation
0	LRC Bit 1	LRC register output Bit 1.
1	LRC Bit 2	LRC register output Bit 2.
2	LRC Bit 3	LRC register output Bit 3.
3	LRC Bit 4	LRC register output Bit 4.
4	LRC Bit 5	LRC register output Bit 5.
5	LRC Bit 6	LRC register output Bit 6.
6	LRC Bit 7	LRC register output Bit 7.
7	LRC Bit P	LRC register output Bit P.

After a successful read or write, the content of the LRC register should be all zeros. One bits indicate error in the corresponding channel. LRC register will be precleared on any I/O operation other than Sense or Monitor Sense operation.

Inter Computer Control Unit (ICCU)

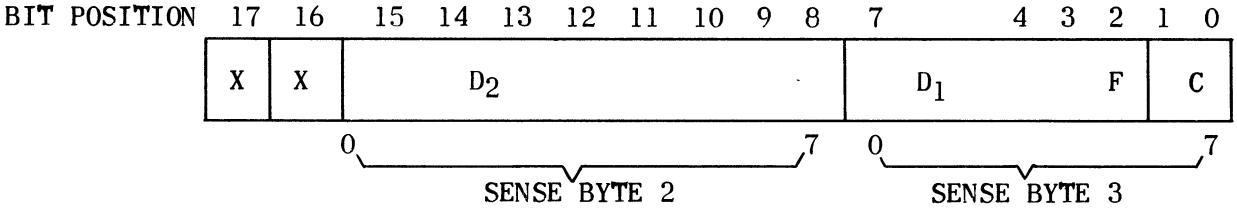
1. COMMAND REPERTOIRE

1.1 CONTROL COMMANDS

These commands are provided so that the Master and Slave can communicate to a limited extent without setting up Data Buffers. When one of these Commands is issued an External Interrupt Request is transmitted to the opposite interface and the COMMAND itself is made available to the opposite interface as External Interrupt Status or Sense bytes.

1.2 MASTER EXTERNAL FUNCTION WORD FORMAT

The Format for bits 0—17 of the EF word from the Master is shown below:



Field	Bits	Function
X	17,16	These bits are ignored
D_2	15-8	Detail, transmitted to the slave in Sense Byte 2. Not interpreted by ICCU.
D_1	7-4	Detail, transmitted to the slave with F and C in Third Sense Byte. Not interpreted by ICCU.
F	3,2	DATA FORMAT SELECTION F = 00 Select Format A F = 01 Select Format B F = 1X Select Format C
C	1,0	CONTROL FIELD 01 INPUT Transmit data to Master 10 OUTPUT Call for data from Master 00 Set "Attention" Interrupt Request to Slave. No data is transferred. 11 Invalid (Automatic No-Match)

1.3 SLAVE COMMAND FORMAT

	COMMAND BYTE	FUNCTION
1.3.1	XX00 0000	TEST I/O No operation, supply status to slave.
1.3.2	XX01 0000	SET INHIBIT STATUS This command is processed as a TEST I/O. (If accepted, it does not generate new status.) The Status Byte is presented to the channel and INHIBIT STATUS IN (Bit 6 of Sense Byte) is set.
1.3.3	XX10 0000	RESET INHIBIT STATUS Same action as SET INHIBIT STATUS, except Bit 6 of Sense Byte is reset.
1.3.4	XXXX 0100(1)	SENSE Transmit 4 bytes of Sense data to Slave. The 2nd and 3rd bytes are taken from the Word Register, bits 0-7 and 8-15. This provides a means of transmitting 16 bits of the EXTERNAL FUNCTION word from Master to Slave. The first byte is detail for the Unit Check Status. The 4th byte has the same format as bits 16-9 of the Master Interrupt Status Word.
1.3.5	DDDD DD10(1,2)	INPUT Transmit data to Slave.
1.3.6	DDDD DD01(1,2)	OUTPUT Call for data from Slave.
1.3.7	DDDD DD11(1,2)	SET EXTERNAL INTERRUPT REQUEST No Data Transfer, Send External Interrupt Request to Master, with the 8-bit Command code on Master Input Data Lines 0-7.

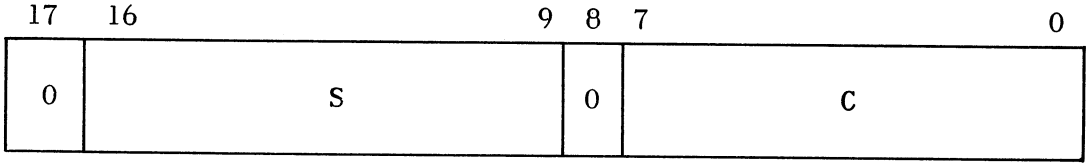
NOTE (1) If the ICCU is "off-line" to the Master computer, bits 0 and 1 of these commands will serve in place of the "F" field of the Master EF word and will control the format. (Bit 0 will be equivalent to Bit 3 of the Master EF word.)

NOTE (2) X Bits and D Bits are not interpreted by the ICCU except as specified in Note (1). D Bits are passed on to the Master via an External Interrupt Word.

2. STATUS BYTES

2.1 EXTERNAL INTERRUPT STATUS WORD

When External Interrupt Request is transmitted to the Master, the data in I/O Input lines 17-0 will be as follows: (Bits above 17 on larger interfaces will be zeros.)



Bits	Field	Description
17		Always zero.
16-9	S	The same Format as Sense Byte 4. Bit 16 corresponds to bit 0 of the Sense byte.
8		Always zero.
7-0	C	The Command Byte from the Slave when the Slave has issued a command other than SENSE I/O or a TEST I/O. All zeros on termination of data transfer.

2.2 SLAVE STATUS BYTE

	Bit	Designation	Interpretation
2.2.1	0	ATTENTION	The Master has issued a Control Command to the ICCU, or the Master has issued the First command and a Slave Command is required to initiate data transfer. When the ATTENTION interrupt has been generated, the Slave must issue a Sense Command in order to examine the Master EF Word. Hardware restrictions will cause all subsequent commands to be rejected if the Sense Command is not issued.
2.2.2	1	Status Modifier	Used only on C.U. Busy Sequence
2.2.3	2	Not used	
2.2.4	3	Busy	Indicates the Control Unit cannot accept a command because: 1) It is executing a previously initiated I/O operation; STATUS MODIFIER also is set. The Control Unit is defined as Busy from the time a command from the Channel is loaded into the Command Register until both CHANNEL END and DEVICE END are set. 2) The Control Unit is holding pending status conditions detected subsequent to completion at the last data transfer command. (Not applicable to TEST I/O or SET/RESET Inhibit Status.)

SLAVE STATUS BYTE (cont)

	Bit	Designation	Interpretation
2.2.5	4	Channel End	Always occurs with DEVICE END.
2.2.6	5	Device End	A Data Transfer was terminated or a Control Command was accepted. (Control Commands are Control Immediate type.)
2.2.7	6	Unit Check	Set simultaneously with bits 0-5 in Sense Byte 1.
2.2.8	7	Unit Exception	Set whenever an EF is received from the Master during a data transfer, i.e., Master Termination.

3. SENSE BYTE FORMATS

The Slave computer may accept 0, 1, 2, 3, or 4 SENSE BYTES as desired;

3.1 Sense Byte 1

Bit	Designation	Interpretation
0	Command Reject	Unspecified command issued to ICCU. This indication (to slave) is suppressed if command byte has incorrect parity.
1	Not used	Transmitted as zero.
2	BUS OUT Check	Even parity on BUS OUT during transfer of data or command to ICCU from Slave channel.
3	Not used	Transmitted as zero.
4	Not used	Transmitted as zero.
5	Not used	Transmitted as zero.
6	Inhibit STATUS IN FF state	"1" whenever the FF is set.
7	Not used	Transmitted as zero.

3.2 Sense Byte 2

(Refer to paragraph 1.2)

3.3 Sense Byte 3

(Refer to paragraph 1.2)

3.4 Sense Byte 4

	Bit	Designation	Interpretation
3.4.1	0	Selective Reset	An operation has been terminated by the Slave with Selective Reset (Error detected by Slave Channel).
3.4.2	1	Master Termination	An operation has been terminated by the Master before normal completion. (Will always be a "0" to SENSE COMMAND. Status FF7 is set by same condition.)
3.4.3	2	Not used	Always transmitted as zero.
3.4.4	3	Bus Parity Error	A parity error has been detected on the Slave OUTPUT BUS. (Will always be a "0" to SENSE Command. Bit 2 of first SENSE BYTE is set by the same condition).
3.4.5	4	Format Reg. FF2	Same as Bit 3 of last Master EF Word. If Master is off-line then same as Bit 0 of Slave SENSE Command byte.
3.4.6	5	Format Reg. FF1	Same as Bit 2 of last Master EF Word. If Master is off-line then same as Bit 1 of Slave SENSE Command byte.
3.4.7	6	Master Function Reg. FF2	Same as Bit 1 of last Master EF Word.
3.4.8	7	Master Function Register FF1	Same as Bit 0 of last Master EF Word.

UNIVAC 9000 Series 900/1100 LPM
Drum Printer and Control

1. Command Repertoire

1.1 The following command codes may be issued to the Printer Control Unit by the processor. Any other codes will be rejected and will return a Unit Check Status to the processor with the Command Reject bit (0) set in the Sense Byte.

	Command	Code	Description
		P01234567 P = Odd Parity Bit X = Ignored by Control Units CDEF = Detail Bits	
1.2	Test I/O	PXX110000 or PXX000000	The Control Unit transmits the Status Byte to the channel. SERVICE OUT from the channel resets (clears) the Status.
1.3	Set Inhibit Status	PXX010000	This command is processed as a Test I/O Command (if accepted, it does not generate any new status). Status will be presented to the channel and the Inhibit Status In Flip-Flop (FF) will be set.
1.3.1			The condition of the Inhibit Status In FF can be examined in Sense Byte 1, bit position 6. When Inhibit Status is set, the Printer Subsystem will not initiate any sequences to present status. The Set Inhibit Status Command should not be issued if the Printer Subsystem is connected to a Selector channel.
1.4	Reset Inhibit Status	PXX100000	This command is processed as a Test I/O Command (if accepted, it does not generate any new status). Status will be presented to the channel and the Inhibit Status In FF will be reset.
1.5	Sense I/O	P00000100	The Printer Control Unit transfers the Sense Byte to the channel as input data. The Sense Byte generally supplies details about any unusual conditions that occured during the last operation.
1.5.1			The Sense Byte is cleared upon receipt of a valid new command code but is not altered by a Sense or Test I/O command. In addition to supplying pertinent information to the Program, this data can be used as maintenance aids.

	Command	Code	Description
1.6	Print (Write)	P01234567 P0CDEF001	(Print and Advance):* Data Characters for one print line are transferred by the channel to the printer buffer; the line is printed; and the paper is then advanced to the next print line. From 0 to 132 characters may be transferred for printing; loading of the buffer begins with Column 1 and continues sequentially until 132 characters have been loaded or until the channel indicates end of data transfers, whichever occurs first. In the latter case, the Control Unit fills the remaining buffer positions with the selected non-printing code. *NOTE: The buffer can be loaded during a previous Advance Paper so as to maintain the maximum print rate. Time to load the buffer is 800 μs nominal CDEF Detail Bits are defined under Forms Control.
1.7	Advance-No Print (Control)	P0CDEF011	This code is used for non-data transfer operations in the printer control unit. The paper is advanced, without printing, to the position specified by the detail bits,,C, D, E, and F.
1.8	Read (Diagnostic)	P00000010	The Read command will first transfer the contents of the 132 byte buffer loaded by a previous print command followed by the 64 byte buffer loaded by the Load Code command.
1.9	Load Code	P11111011	The Load Code command loads a 64 byte buffer with a 6, 7, or 8 bit code that represents the code for the characters on the print drum. This command enables code conversion by the printer. The sequence of loading must be as follows: (Corresponds to the ordering on the print drum).

1.	&	17.	L	33.	2	49.	>	(greater than)
2.	Z	18.	F	34.	3	50.	<	(less than)
3.	K	19.	H	35.	4	51.	;	
4.	J	20.	S	36.	5	52.	:	
5.	Q	21.	R	37.	6	53.	¢	
6.	X	22.	0	38.	7	54.	|	(absolute)
7.	V	23.	A	39.	8	55.	¬	(logical not)
8.	W	24.	N	40.	9	56.		(underline)
9.	Y	25.	I	41.	*	57.	"	(quote)
10.	P	26.	T	42.	/	58.	!	
11.	G	27.	E	43.	+	59.	?	
12.	B	28.	.	44.	$	60.	\	
13.	U	20.	, (comma)	45.	(	61.	%	
14.	M	30.	- (minus)	46.	)	62.	#	
15.	C	31.	0	47.	=	63.	@	
16.	D	32.	1	48.	' (apost.)	64.	Non-printing (space)	

	Command	Code	Description
1.10	Forms Control	POCDEF001 (Print) or POCDEF011 (No-Print)	This data is transferred as part of a Print or Advance—No Print command. Paper is spaced as specified in detail bits CDEF as follows:

P01234567

CDEF	Machine A	Machine B
0000	No Advance	No Advance
0001	Advance 1 line	Advance 1 line
0010	Advance 2 lines	Advance 2 lines
0011	Paper Loop Control*	Advance 3 lines
0100	↓	Paper Loop Control*
thru		↓
1110		Home Paper Loop Control 6 lines/inch
1111	Home Paper Loop Control	Home Paper Loop Control 8 lines/inch

*Paper is advanced under control of the Forms Control tape loop to the line corresponding to the same hole combination in the loop. The Skip may be from 1 to 132 lines maximum.

1.11 "Home Paper" Codes

1.11.1 By programming convention, the codes "1110" and "1111" in the Forms Control tape loop are reserved for "Home Paper". They require no special recognition in the Control Unit.

Home Paper Command Bits	CDEF
Paper Loop Bits	8421
Machine A	1111
Machine B	1110 6 lines/inch
Machine B	1111 8 lines/inch

1.11.2 On Machine B the 6/8 LPI Switch is deleted. For initial set-up, or whenever the loop is changed, the Home Paper Switch is depressed twice before paper is loaded. Thereafter it need only be depressed once. The Home Paper Indicator lights whenever in the Home Paper position. A paper tape loop must always be used with the Home Paper punched in it.

1.11.3 On Machine B, when Forms Out occurs, there may still be 2-1/2 inches of paper left. The Forms Out condition will not be indicated until the home paper position is detected by the loop control photocells. The paper advance portion of the instruction just completed will continue to advance to the location called for in that instruction. The current print or space command will be inhibited at this time and "STOP" and "FORMS OUT" will be set. The operator may now line up the new forms with the last one in the machine.

1.12 Form Overflow

1.12.1 By programming convention, the code "1001" punched in the Forms Control tape loop is reserved to specify "end of form". If this code is detected during a Control or Write command-initiated form advance, either single or double spaced, the Control Unit:

1. Terminates the operation and does not execute a pending Print or Advance-No Print command which may have been initiated by the channel after printing the previous line but prior to the completion of paper advance.

2. Sets the Unit Exception bit (7) in the Status Byte which will be transmitted to the channel at Device End of this command or Initial Selection of the next command.

2. Status Byte

2.1 The Status Byte contains information on the status of the printer and Control Unit and some data on conditions of the last operation. It is presented to the Channel at these times:

1. End of the Initial Selection Sequence.
2. At the end of data transfers for the Print, Read, and Load Code commands.
3. Completion of printing a line and start of paper advance for the current print command.
4. At the start of paper advance for the Advance-No Print command. Normally, it is not presented at the end of paper advance.

2.2 The Status Register in the Control Unit is cleared when the channel responds to STATUS IN with SERVICE OUT. The bits in the Status Byte are defined as follows:

	Bit Position	Designation	Interpretation
2.3	P	Odd Parity	Parity for Status Byte
2.4	0	Attention	Machine A - Not used, always "0". Machine B - This bit will be set whenever the machine is ready, but in the "STOP" condition, and "RUN", is depressed. The Attention Bit is an operator-controlled interrupt indicating that the machine has gone from an inactive to an active state.
2.5	1	Status Modifier	Present with Busy to indicate the printer is busy executing a previously initiated operation.
2.6	2	Control Unit End	Not used, always "0".
2.7	3	Busy	Indicates that the printer cannot accept a command because one of the following conditions exists: a. Printer is executing a previously initiated command (Bit 1, Status Modifier, will also be present). b. Printer is holding pending status conditions from a previous command (not applicable to Test I/O or Reset or Set Inhibit Status).
2.8	4	Channel End*	Presented at the end of data transfer on a Print command.
2.9	5	Device End*	Indicates the completion of a command accepted by the printer, exclusive of paper advancement. It is presented in these cases: 1. At the completion of printing the line and start of paper advance. 2. At the start of paper advance for an Advance-No Print command. 3. At the completion of a Sense, Read, or Load Code command.
2.10	6	Unit Check	Set when any bit but 6 in the sense byte is set, except during a Sense command when bit 7 of the Sense byte is set.
2.11	7	Unit Exception	Indicates a Form Overflow condition from the end-of-paper detector. Presented with Device End on those commands which initiate paper advance.

*Presented simultaneously at the completion of Sense, Read, and Load Code commands, and at the beginning of the paper advance for the Advance-No Print command.

3. Sense Data Bytes

3.1 The Sense Data Bytes provide information about unusual conditions occurring during the last operation. The Sense Bytes are cleared when the next valid command code is accepted by the Control Unit.

3.2 Sense Byte 1

	Bit Position	Designation	Interpretation
3.2.1	P	Odd Parity	Parity for Sense byte.
3.2.2	0	Command Reject	An invalid command was issued by the channel.
3.2.3	1	Intervention Required	Paper low or paper runaway.*
3.2.4	2	BUS OUT CHECK	Parity error on a command or data transfer to the Control Unit. Parity error on command codes causes immediate termination; on data transfers. no immediate termination.
3.2.5	3	Equipment Check	Indicates an equipment malfunction during last printing operation.
3.2.6	4	Data Check	Buffer Parity error.
3.2.7	5	Overrun	Print not completed in 1 revolution.
3.2.8	6	Inhibit Status	Inhibit Status is set.
3.2.9	7	Not Ready	Indicates the Printer and/or Control Unit is not operative. This bit is set whenever one of the conditions described below is encountered.

*A runaway paper condition can arise if the Forms Control code is not punched into the paper tape loop or from malfunctioning of the paper advance mechanism. The Control Unit contains circuitry which will stop the paper automatically approximately 1.2 seconds after the start of an advance (unless it stops before that time). If this contingency stop is reached, the runaway paper bit in the Sense byte and the Unit Check bit in the Status byte are set. A pending "Print" or "Advance-No Print" command in the Control Unit is suppressed.

Not-Ready Conditions

Machine A	Machine B
1. Power Check	1. Power Check
2. Interlock	2. Interlock
3. Temperature Ck.	3. Temperature Ck.
4. Print Check	4. Print Check
5. Ribbon Check	5. Ribbon Check
6. Carriage Out	6. Carriage Out
7. Forms Runaway	7. Forms Runaway
	8. Parity Check
	9. Forms Out

3.3 Sense Byte 2

	Bit Position	Designation	Interpretation
3.3.1	P	Odd Parity	Parity for Sense Byte.
3.3.2	0	Buffer Parity Error, Code	Indicates a Buffer Parity Error in the code area only.
3.3.3	1	Buffer Parity Error, Data	Indicates a Buffer Parity Error in the data area only.
3.3.4	2	Once per Revolution Error	Indicates Counter is not equal to 63 when the once per revolution pulse occurs.
3.3.5	3	Sprocket Error	Indicates a data pulse identical on two consecutive sprocket pulses.
3.3.6	4	Scan Error	Next sprocket occurred before the Scan Cycle was completed.
3.3.7	5	Early Terminate	The Channel terminates data transfers on any command. Status flip-flop 6 is set on Load Code only.
3.3.8	6	Paper Low	Machine A - Indicates the Printer is running out of paper (Forms Out). Machine B - a. Depression of "STOP" will set this bit and the Unit Check Bit, Status Bit 6. This is an operator-action stop. All stops occur at the completion of the current instruction. b. Any non-ready condition, or error condition, will also set Sense Byte 2, Bit 6 and Unit Check and will be further defined in the Sense Bytes. c. The Test, Sense, Read, and Load Code commands can be performed when in the "STOP" mode. The Read and Load Code command cannot be performed on certain "STOP" conditions, such as Power, Interlock and Temperature Check.
3.3.9	7	Selective Reset/ Interface Disconnect	This Bit is set if a Selective Reset/Interface Disconnect Sequence occurred anywhere since the last Sense Command was issued.

Perforated Tape Subsystem for the
DCT 2000 and the 9000 Series

1. Command Code

1.1 The basic format for the Command byte transferred from the Channel to the Controller during the Initial Selection Sequence is shown below.

COMMAND		BIT POSITION
		P 0 1 2 3 4 5 6 7
Test		P X X 0 0 0 0 0 0
	OR	P X X 1 1 0 0 0 0
Set Inhibit Status		P X X 0 1 0 0 0 0
Reset Inhibit Status		P X X 1 0 0 0 0 0
Sense		P 0 0 0 0 0 1 0 0
Punch		P 0 0 0 0 0 A 0 1
Read		P 0 0 0 0 0 A 1 0
Control		P 1 0 0 0 0 0 1 1

P = Odd Parity Bit
A = 1, ignore control codes, operate binary mode
A = 0, character recognition is operative
X = to be ignored by the Controller

Any other Command Code shall be treated as an invalid Command by the Controller. Issuance of a PUNCH or READ Command in the absence of the associated feature on the subsystem shall constitute an invalid command.

1.2 Test. This Command Code shall cause transfer of the Controller Status Byte to the Channel. This command will not cause any new status indications to be generated.

1.3 Set Inhibit Status. This command is processed as a Test Command. Status will be presented to the Channel and Inhibit Status In will be set.

1.4 Reset Inhibit Status. This command is processed as a Test Command. Status will be presented to the Channel and Inhibit Status In will be reset.

1.5 Sense. This Command Code shall cause the Controller to transfer, as input data, up to two bytes of sense indication to the Channel.

1.6 Punch. This Command Code shall initiate the punching of one block of data on the Punch. The block is terminated when the Channel responds to SERVICE IN with COMMAND OUT.

1.7 Read. This Command Code will initiate the reading of one block of data from the Reader.

1.8 Control. This Command Code is reserved for Failure Finding. Non-diagnostic programs should not attempt to set up this Command Code.

2. Status Byte

2.1 The Controller shall automatically place a STATUS Byte on the input bus to the Channel before signaling a STATUS IN. The format of the STATUS Byte is as follows:

BIT	STATUS
P	Odd Parity Bit
0	Attention
1	Status Modifier
2	Not Used
3	Busy
4	Channel End
5	Device End
6	Unit Check
7	Unit Exception

2.2 Attention. Either Reader or Punch has changed from STOP to RUN mode. (Control panel push-button.)

2.3 Status Modifier. This bit is normally set along with the Busy Status Bit. Status Modifier will not be set with Busy if a new Command is issued to the Controller when it is about to initiate an interrupt to present end status from the previous operation.

2.4 Busy. This bit is transmitted during the Control Unit Busy sequence. "Busy" is also transmitted when a command other than TEST is attempted and the Controller has status pending from a previous operation.

2.5 Channel End. This bit is set whenever a data block is terminated. It is also set during Initial Selection when a CONTROL command is accepted and no data is to be transferred. Channel End will always be presented with Device End.

2.6 Device End. This bit is set when the Reader or Punch completes an I/O Operation. Device End will always be presented with Channel End.

2.7 Unit Check. Unit Check will be presented when a read command is issued and a reader fault exists and when an error or fault is encountered after a command is initiated. Any bit in sense byte 1 will set Unit Check.

2.8 Unit Exception. Unit Exception will be presented if a STOP CHARACTER is detected on Read.

3. Sense Bytes

3.1 Sense Byte Ø

BIT	INDICATION
P	Odd Parity Bit
0	Command Reject
1	Intervention Required
2	Bus Out Check
3	Equipment Check
4	Data Check
5	Not Used
6	Inhibit Status Set
7	Tape Fault

3.1.1 Command Reject. The Command Code received is invalid.

3.1.2 Intervention Required. Manual or program intervention is required to clear the Controller or the Reader/Punch of a condition which prevents future operation, such as:

(r.p.) Program connector not inserted
(p) Punch Take-up reel full
(r) Broken tape in reader
(r) End of tape in reader
(p) Low Tape on Punch
(r) Reader in Stop Mode
(p) Punch in Stop Mode

3.1.3 Bus Out Check. Bus Out Check sets when a parity error has occurred.

(p) Does not punch the bad character if in punch data
(rp) Parity error on instruction transfer or last data character.

3.1.4 Equipment Check. A read error, broken tape, or overshoot condition exists on the Reader. A low paper tape supply condition exists on the Punch.

3.1.5 Data Check. A read parity error has been detected. Data is read until the Channel terminates data transfers.

3.1.6 Inhibit Status. Inhibit Status FF set.

3.1.7 Tape Fault. indicates:

(r) Normal End of Tape
(p) Low Tape Supply

3.2 Sense Byte 1

BIT	INDICATION
P	Odd Parity Bit
0	Reader STOP FF
1	Punch STOP FF
2	Program Connector not inserted
3	Not used.
4	Punch Take-up reel full
5	Low tape supply on Punch
6	Broken tape on Reader
7	Normal End of Tape on Reader

DCS 1, 4

Data Communications Subsystems

1. Command Byte Repertoire - Table A lists the commands accepted by the DCS from the channel. Table B lists the bit configurations of these commands when they are encoded by the LTC and accepted by the line terminals.

2. Status Byte - The Status Byte indicates to the processor the operational condition of the DCS and initiates processor I/O interruption for a variety of reasons, such as the receipt of an invalid sequence of commands. When an abnormal or error condition exists in the DCS, a Unit Check Status Byte is sent to the processor. After the processor returns the required Sense command, additional information is sent to the processor in two Sense Bytes, indicating the specific nature of the abnormal condition.

2.1 Status Byte Repertoire - Table C lists the Status Bits generated by the DCS.

3. Sense Bytes - The Sense Bytes are used by the DCS when it is necessary to convey additional information to the processor. When an error condition arises in the DCS, a Unit Check Status Byte is sent to the processor. The processor replies with a Sense Command. The DCS then presents the more detailed information in two Sense Bytes.

3.1 The DCS always transmits two Sense Bytes to the processor. The Input LT encodes both Sense Bytes. The Output LT encodes the first Sense Byte and can encode the second Sense Byte when a Dialing Adapter is attached (Dial No Good).

3.2 Tables D and E itemize the first and second Sense Byte bit-indicators generated by the DCS.

Table A. Command Byte Repertoire

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
WRITE Send Data	P 0 0 0 0 0 0 0 0 1	A command sent during an Initial Selection Sequence which starts the Output Data Sequence and causes the LT to generate an all-zeros Status Byte as a response.	-00, -02, & -06.	-00 & -02.	-00, -02, & -04.	
Dial	P 0 0 0 0 0 1 0 1	Same as Send Data. Only accepted by an Output LT equipped with a Dialing Adapter (F1007-00). Output LT does not perform the dialing function. A Turn-On Command Byte must be sent to the Input LT before sending a Dial Command Byte to the Output LT.	-00, -02, & -06.	-02.	-00, -02, & -04.	
Send Break	P 0 0 0 1 0 0 0 1	A command sent to an Output LT which causes the CI (F1002-09) to send a break (spacing) signal for a minimum of 205 ms. The command also causes the CI (F1002-10) to send a break (spacing) signal for one second. The break is normally used to stop a remote transmitter. This command causes the LT to generate an all-zeros Status Byte as a response.	-06.			

Table A. Command Byte Repertoire (cont)

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
READ Turn-On	P 0 0 0 0 0 0 1 0	A command sent during an Initial Selection Sequence which starts an Input Data Sequence and causes the LT to generate an all-zeros Status Byte as a response. When data is available on the Input Data lines, it will be transmitted to the processor. This command is also used by the F1002-04, -06, or -09 CI to accept an incoming call following the receipt of the RING INDICATOR signal, or it is used to condition the CI to permit a Dial function to be performed.	-01, -03, & -07.	-01 & -03.	-01, -03, & -05.	-01.
New Sync	P 0 0 0 0 1 0 1 0	A command accepted by an Input LT which controls the CI (F1002-03 & -04 only) and enables it to quench the receive clock of a synchronous modem. This causes fast resynchronization with a newly turned-on remote transmitter and causes the Input LT to generate an all-zeros Status Byte as a response. This command is normally used for multiple-party connections only.			-01, -03, & -05.	

Table A. Command Byte Repertoire (cont)

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-L F1004-XX	LT-S F1005-XX	LT-P F1006-XX
READ (cont) Look-For Sync (LFS) or Parallel Test	P 0 0 0 0 0 1 1 0	A command which nullifies character synchronization in an Input LT-S and then causes the LT-S to identify two contiguous unique Sync Characters and a non-sync character (SOM Character is optional) out of a serial data stream. New character synchronization is then established. This command also causes the Input LT-S to stop sending data. The LT-S begins sending data only when a non-sync character (SOM or Data Character) is received following re-synchronization. This command causes the Input LT-S to generate an all-zeros Status Byte as a response. Parallel Test provides the LT-P with back-to-back testing capability (used only during the DCS Test mode). It is the final command transmitted by the processor and immediately follows a DCS Test and a Turn-On command.			-01, -03,	-01

Table A. Command Byte Repertoire (cont)

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
READ (cont)						
Answer Back A Answer Back B Answer Back AB	P 0 0 0 1 0 0 1 0 P 0 0 0 1 0 1 1 0 P 0 0 0 1 1 0 1 0	A command sent to the Parallel LT which allows the CI (F1002-07) to send three different tones on the ANSWER-BACK channel of the 403D5 or 403D6 Data Set. The processor can select and control these tones via the coding within the command. The select-tone is sent for three to five seconds. This command causes the Parallel LT to generate an all-zeros Status Byte as a response.				-01.
CONTROL						
Turn-Off	P 0 0 0 0 0 0 1 1	A command which causes the immediate termination of an Input or Output Data Sequence and causes the LT to generate a Channel End - Device End Status Byte as a response.	-00, -01, -02, -03, -06, & -07.	-00, -01, -02, & -03.	-00, -01, -02, -03, -04, & -05.	-01.
DCS Test	P 0 0 0 0 1 0 1 1	A command to the Input LT which terminates the connections between the CI and the communications lines or modem and causes the Input LT to generate a Channel End - Device End Status Byte as a response. This command connects the output signal to the input signals for loop-back testing of the DCS by the processor.	-01, -03, & -07.	-01 & -03.	-01, -03, & -05.	-01.

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SPECIFICATION SHEET

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Table A. Command Byte Repertoire (cont)

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
CONTROL (cont) End Test	P 0 0 0 0 1 1 1 1	A command to the Input LT which switches the CI back to normal operation following a DCS or Local Test operation and causes the Input LT to generate a Channel End - Device End Status Byte as a response.	-01, -03, & -07.	-01,& -03.	-01, -03, & -05.	-01.
Disconnect	P 0 0 0 1 0 0 1 1	A command to the CI (F1002-04, -06, or -09) via the Input LT for the purpose of terminating a call. Upon receipt of the signal, the DATA TERMINAL READY signal is dropped to the modem, indicating a "hang-up". This command causes the Input LT to generate a Channel End - Device End Status Byte as a response.	-01, -03, & -07.	-01,& -03.	-01, -03, & -05.	-01.
Local Test	P 0 0 0 0 0 1 1 1	A command to the Input LT which causes the CI (F1002-05) to exercise the Local Test Control on the associated modem. This command places the modem in the loop-back test mode for testing all local (on-site) hardware including the modem. (Applies only to modems which have turn-around capability.) This command causes the Input LT to generate a Channel End - Device End Status Byte as a response.	-01, -03, & -07.	-01 & -03.	-01, -03, & -05.	

Table A. Command Byte Repertoire (cont)

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
SENSE	P 0 0 0 0 0 1 0 0	When an error condition exists in the DCS, the appropriate line terminal sends (via the LTC) a Unit Check Status Byte to the processor. The processor then replies with a Sense command. The Sense command tells the line terminal to return an all-zeros Status Byte followed by two Sense Bytes.	-00, -01, -02, -03, -06, & -07.	-00, -01, -02, & -03.	-00, -01, -02, -03, -04, & -05.	-01.
TEST I/O	P 0 0 0 0 0 0 0 0	A command which is used to obtain the present status of a line terminal. This command does not cause the generation of new status but does cause the LT to generate an all-zeros Status Byte as a response.	-00, -01, -02, -03, -06, & -07.	-00, -01, -02, & -03.	-00, -01, -02, -03, -04, & -05.	-01.

Table B. Bit Configurations of LTC Encoded Command Bytes

Title of Command	Bit Configuration P 0 1 2 3 4 5 6 7
Send Data	P 0 0 0 0 0 1 0 1
Dial	P 0 0 0 0 1 0 0 1
Send Break	P 0 1 0 0 0 0 0 1
Turn-On	P 0 0 0 0 0 1 1 0
New Sync	P 0 0 0 1 0 0 1 0
Look-For-Sync (LFS)/ Parallel Test	P 0 0 0 0 1 0 1 0
Answer Back A	P 0 1 0 0 0 0 1 0
Answer Back B	P 1 0 0 0 0 0 1 0
Answer Back AB	P 0 0 0 1 0 0 1 0
Turn-Off	P 0 0 0 0 0 1 1 1
DCS Test	P 0 0 0 1 0 0 1 1
End Test	P 0 0 1 0 0 0 1 1
Disconnect	P 0 1 0 0 0 0 1 1
Local Test	P 0 0 0 0 1 0 1 1
SENSE	P 0 0 0 0 0 1 0 0
TEST I/O	P 0 0 0 0 0 1 0 0

Table C. Status Byte Repertoire[1]

Title of Status	Bit Configuration P 0 1 2 3 4 5 6 7	Description
Busy	P 0 0 0 1 0 0 0 0	This status condition is generated by an Output or Input LT and tells the processor that a previously initiated command is in progress.
Channel End	P 0 0 0 0 1 0 0 0	Same as Device End.
Device End	P 0 0 0 0 0 1 0 0	This status condition is generated by an Output or Input LT and tells the processor that a previously initiated command is completed.
Unit Check	P 0 0 0 0 0 0 1 0	This status condition is generated by an Output or Input LT and tells the processor that an abnormal or error condition exists. It also tells the processor to send a Sense Command if additional information on an error or status condition is required.
Unit Exception	P 0 0 0 0 0 0 0 1	This status condition is generated by the LTC and indicates a non-existent or inactive line terminal.

[1]All Status Bytes are applicable to all line terminals.

Table D. First Sense Byte Repertoire

Title of Sense	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
Command Reject	P 1 0 0 0 0 0 0 0	Indicates an invalid Command Byte was presented to either an Input or Output LT.	-00, -01, -02, -03, -06, & -07.	-00, -01, -02, & -03.	-00, -01, -02, -03, -04, & -05.	-01.
Bus Out Check	P 0 0 1 0 0 0 0 0	Indicates a parity error exists in a Command Byte. This error condition is detected by the LTC.	-00, -01, -02, -03, -06, & -07.	-00, -01, -02, & -03.	-00, -01, -02, -03, -04, & -05.	-01.
Data Check	P 0 0 0 0 0 1 0 0	Indicates a parity error existed on a Data Byte in the previous Data Block. This error condition is detected by the LTC and only applies to Output LT's.	-00, -02, & -07.	-00, & -02.	-00, -02, & -04.	
Overrun (Data Late)	P 0 0 0 0 0 0 1 0	Indicates data was late in being acknowledged or sent by the processor.	-01, -03, & -07.	-01, & -03.	-00, -01, -02, -03, -04, & -05.	-01.
Ring Indicator	P 0 0 0 0 0 0 0 1	Indicates that a ringing signal is being received from a remote station. A Turn-On Command Byte must then be sent to the Input LT. The DCS will answer calls automatically. This particular condition only applies to an Input LT.	-03, & -07.	-03.	-01, -03, & -05.	-01.

Table E. Second Sense Byte Repertoire

Title of Sense	Bit Configuration P 0 1 2 3 4 5 6 7	Description	Applicable Line Terminals			
			LT-L F1003-XX	LT-M F1004-XX	LT-S F1005-XX	LT-P F1006-XX
Message Status (LRE) Longitudinal Redundancy Error	P 1 0 0 0 0 0 0 0	Indicates a message (or block) parity error is detected. This condition only applies to an Input LT.		-03.	-03, & -05	
Message Status (CPE) Character Parity Error	P,0 1 0 0 0 0 0 0	Indicates a Data Character (or Data Byte) parity error is detected in a message (or block). This condition only applies to an Input LT.	-03, & -07.	-03.	-03, & -05.	
Error - Carrier OFF (AGC Lock)	P 0 0 1 0 0 0 0 0	Indicates loss of carrier when receiving a message (the INPUT DATA signal has dropped). This condition only applies to an Input LT.	-03, & -07.	-03.	-03, & -05.	
Dial No Good	P 0 0 0 1 0 0 0 0	Indicates no connection established after a Dial command is send. Only generated by an Output LT connected to a Dialing Adapter (F1007-00).	-00, -02, & -06.	-00, & -02.	-00, -02, & -04.	
Time-Out (180 ms) Break	P 0 0 0 0 0 1 0 0	Indicates the Input LT has received a BREAK signal from a station on the TWX network. A BREAK signal is a spacing signal held for 180 ms duration. The BREAK signal is sent by a remote station for the purpose of stopping a transmitter. When operating in a TELEX network, the BREAK signal indicates a disconnection.	-07.			

FUNCTION CODES

U12/U16 Control Unit No. 5017-XX

Command	0	1	2	3	4	5	6	7
TEST	X	X	0 1	0 1	0	0	0	0
SET INHIBIT STATUS	X	X	0	1	0	0	0	0
RESET INHIBIT STATUS	X	X	1	0	0	0	0	0
SENSE	0	0	0	0	0	1	0	0
SENSE/RESERVE	1	1	1	1	0	1	0	0
SENSE/RELEASE	1	1	0	1	0	1	0	0
WRITE	0	0	0	0	0	0	0	1
READ	0	0	0	I	0	0	1	0
READ BACKWARD	0	0	0	I	1	1	0	0
CONTROL	0	0	C	C	C	1	1	1
MODE SET	D	D	M	M	M	0	1	1

X, I = 1 or 0 bit

CCC (Control Code)

000 = REWIND
001 = REWIND WITH INTERLOCK
010 = ERASE
011 = WRITE TAPE MARK
100 = BACKSPACE BLOCK
101 = BACKSPACE FILE
110 = FORWARD SPACE BLOCK
111 = FORWARD SPACE FILE

DD (Density Set)

00 = 200 bpi
01 = 556 bpi
10 = 800 bpi
11 = Set 9-track Mode

{ 7-track NRZI Operation

DDMMM (Maintenance Mode)

00001 = RESET FAILURE-FINDING MODE
01001 = SET DEVICE SIMULATION MODE
10001 = SET MONITOR MODE

MMM (Mode Modifiers; DD = 11 only)

000 = 1600 bpi Phase Encoding (Reset Condition)
001 = 800 bpi NRZI

MMM (Mode Modifiers; DD ≠ 11 (refer to next page).

NOTE: 9-track operation overrides but does not reset a 7-track mode setting. 7-track operation overrides but does not reset a 9-track mode setting. 9-track operation mode settings apply only to WRITE, WRITE TAPE MARK, or ERASE commands executed from load point.

MMM (Mode Modifiers; DD ≠ 11)

MMM (Mode Modifiers DD ≠ 11)	Set Density	Set Odd Parity	Set Even Parity	Data Converter On	Data Converter Off	Translator On	Translator Off	Request TIE (Track in Error)	Low Gain	
000										NOP (No Operation)
001										Failure-Finding Mode Only
010	x	x		x			x			Reset Condition (Only if Data Converter installed)
011 (DD = 00)								x		9-track only
011 (DD = 01)									x	*
100	x		x		x		x			
101	x		x		x	x				
110	x	x			x		x			Reset Condition (If Data Converter not installed)
111	x	x			x	x				

*The low gain condition will apply to the "READ" or "SPACE" operation immediately following the MODE SET command. At the end of the operation, the mode is reset to normal.

X = Condition set or activated by related mode modifier bit configurations.

UNIVAC

SPECIFICATION SHEET

SHEET 16-3

REVISION -

SPECIFICATION SYMBOL SH04479

U12/U16 Subsystem Type 5017-XX
STATUS, SENSE DATA, MONITOR SENSE DATA, AND SENSE BYTE BIT-DECODE MNEMONICS*

	BIT POSITION	0	1	2	3	4	5	6	7
	STATUS BYTE	ATTENTION	STATUS MODIFIER	CONTROL UNIT END	BUSY	CHANNEL END	DEVICE END	UNIT CHECK	UNIT EXCEPTION
SENSE BYTES	BYTE 0	*CMRJ Command Reject	*INRQ Inter-vention Required	*BSCK Bus Out Check	*EQCK Equipment Check	*DACK Data Check	*OVRN Overrun	*WDCZ Word Count Zero	*SB07 / Data Converter Check *DCCK
	BYTE 1	*NOIS Noise	*TUSA Tape Unit Status "A"	*TUSB Tape Unit Status "B"	*7TRK Seven Track	*BOT Load Point	*EOT End of Tape	*TUFP File Protect	*TUIC Tape Unit Incompatibility
	BYTE 2	*TIE0 TIE0	*TIE1 TIE1	*TIE2 TIE2	*TIE3 TIE3	*TIE4 TIE4	*TIE5 TIE5	*TIE6 TIE6	*TIE7 TIE7
	BYTE 3	*VRC / RWVRC / RVRC / *RVRC	*MDT / MDT / LRC / *LRC	*SKEW SKEW	*PSTC / Postamble / CK / CRC / *CRC	*SDT / SDT / WVRC / *WVRC	*TUPH 1600 Bpi	*BKWD Backward	*SB37 "0"
	BYTE 4	*RWAY Runaway	*TMFT Tape Motion Fault	*SB42 "0"	*SB43 "0"	*SB44 "0"	*STAL Stall	*TPFT Tape Fault	*SB47 "0"
MONITOR BYTES	BYTE 0	*PC00 Prog Count Bit 0	*PC01 Prog Count Bit 1	*PC02 Prog Count Bit 2	*6AV 6AV	*7AV Tape Unit Interface 7AV	*8AV 8AV	*RES Channel Interface Reserved	*SIM Device Simulation Mode Set
	BYTE 1	*WRIT Write	*READ Read	*BKWD Backward	*SPAC Space	*FILE File	*REW Rewind	*WTM Write Tape Mark	*ERAS Erase
	BYTE 2	*PRER Backward Cmd. at LP	*SENT Stop Sentinel Detected	*TMD Tape Mark Detected	*PSTA Inhibit Status Set	*CTRM Early Terminate	*MRPH Erase Mode Set	*DTP DTP CYP *CRCP	*DT0 / DT0 CY0 / *CRC0
	BYTE 3	*DT1 / DT1 CY1 / *CRC1	*DT2 / DT2 CY2 / *CRC2	*DT3 / DT3 CY3 / *CRC3	*DT4 / DT4 CY4 / *CRC4	*DT5 / DT5 CY5 / *CRC5	*DT6 / DT6 CY6 / *CRC6	*DT7 / DT7 CY7 / *CRC7	*PZEP / PZERP LP / *LRCP
	BYTE 4	*PZE0 / PZER0 L0 / *LRC0	*PZE1 / PZER1 L1 / *LRC1	*PZE2 / PZER2 L2 / *LRC2	*PZE3 / PZER3 L3 / *LRC3	*PZE4 / PZER4 L4 / *LRC4	*PZE5 / PZER5 L5 / *LRC5	*PZE6 / PZER6 L6 / *LRC6	*PZE7 / PZER7 L7 / *LRC7

Uniservo 12/Uniservo 16 Subsystem Type 5017

1. Command Repertoire

Command codes not shown and MODE SET or SENSE commands without the corresponding feature in the Control Unit are invalid and will be rejected by the Control Unit. The Command Reject indication sets the UNIT CHECK bit of the status byte.

1.1 TEST (XX000000 or XX110000)

The TEST command initiates the sequence of presenting the status byte to the channel. The STATUS IN pending condition and the status register will be cleared when the status byte is accepted by the channel. TEST commands generate no new status.

1.2 TEST INHIBIT STATUS (XX010000)

This command is performed as a TEST command. In addition, further Control Unit initiated sequences to present status to the channel will be inhibited. This condition remains until reset by a System or Selective Reset, or a RESET INHIBIT STATUS command.

1.3 RESET INHIBIT STATUS (XX100000)

This command is performed as a TEST command. In addition, the Inhibit Status In condition is reset, allowing Control Unit initiated sequences for presentation of status to the channel.

1.4 SENSE (00000100)

The SENSE command stores the current status of the selected tape unit, and then proceeds to transfer the sense bytes to the channel. The information in the sense bytes contains the current status of the tape unit and any error or fault conditions that occurred during the last operation. The status byte presented at the completion of the SENSE command will contain CHANNEL END (Bit 4) and DEVICE END (Bit 5). Any non-ready condition detected in the selected tape unit will not be indicated in the status byte.

1.5 SENSE/RESERVE (11110100)

This command is performed as a SENSE command. In addition, the I/O Interface which issued the command is locked on to the Control Unit. This will prevent operations issued from the other I/O Interface from being initiated until a Reset or a SENSE/RELEASE command is received from the operating interface.

1.6 SENSE/RELEASE (11010100)

1.6.1 This command is performed as a SENSE command. In addition, the reserved state set by the SENSE/RESERVE command, is reset and the Control Unit is free to operate with either I/O Interface. The Control Unit is released when the end status byte for the SENSE/RELEASE command is accepted by the channel.

1.6.2 The actual reserve or release operations are performed during initial selection. After initial selection, the sense operation proceeds as usual. If the reserve and release capability is not utilized, then the first I/O Interface to select the Control Unit will lock on for the duration of the operation.

1.6.3 At the completion of the operation in progress, the Control Unit will be free to operate with either I/O Interface unless:

a. Command chaining is indicated.

b. The end status byte is stacked by the channel.

c. The end status byte contains the UNIT CHECK bit (bit 6).

d. No command other than TEST, SET INHIBIT STATUS, RESET INHIBIT STATUS, or MODE SET (except REQUEST TIE) has been initiated since condition (c) occurred.

1.7 WRITE (00000001)

1.7.1 The WRITE command moves tape on the selected unit in the forward direction. Data is requested from the channel and is written on tape until the channel terminates the data transfer. Writing in the end-of-tape area will cause the UNIT EXCEPTION bit (bit 7) to be included in the end status byte. UNIT EXCEPTION will be set at the completion of the operation in which the end-of-tape marker is detected.

1.7.2 The following description of a normal termination applies for WRITE, READ and READ BACKWARD operations: The end status byte, consisting of the CHANNEL END bit (bit 4) and the DEVICE END bit (bit 5) along with other status bits, if any, will be presented to the channel when the end-of-block is detected on the Read or Check Read. The end-of-block condition is detected when data in all tracks "drops out" for more than 790 μs on a U12 or U6-C, or more than 280 μs on a U16 or U8-C.

1.8 READ (000I0010)

1.8.1 The READ command moves the tape on the selected unit in the forward direction. Data is transferred from the tape and sent to the channel until the end-of-block occurs or the channel terminates the transfer.

The end status byte will include the UNIT EXCEPTION bit (bit 7) if the block read is a tape mark block.

READ (000I0010) (cont)

1.8.2 In NRZI mode, the tape mark character will not be transferred to the channel when detected as a single character tape mark block. However, if the tape mark code appears anywhere in the body of a multiple-character block, it will be transferred to the channel as data. The tape mark in 7-track operations is detected in both even and odd parity modes during "read" and "space" operations.

1.9 READ BACKWARD (000I1100)

1.9.1 The READ BACKWARD command moves the tape on the selected unit in the backward direction and causes a block of data to be read in the reverse order in which it was written on the tape. Data is transferred from the tape and sent to the channel until the end-of-block occurs or the channel terminates the transfer.

Sensing a tape mark is the same as in the READ operation.

1.9.2 Reading backward in 7-track mode should not be attempted with tapes generated on other than U6-C, U8-C, U12, U16, or other tape units which provide scatter correction of the Longitudinal Redundancy Check (LRC) character.

The READ BACKWARD operation in 7-track data conversion mode should not be attempted with tapes having block length other than a multiple of four frames.

1.9.3 The I bit in the read command codes pertains to the Phase Encoding mode of operation only. When this bit is a one, the UNIT CHECK bit (bit 6) will be included in the end status byte if a correctable error occurred during the current read operation (see description of Bit 4, Sense Byte 3, and the Command Code Chart).

1.10 CONTROL (00CCC111)

The CONTROL command involves no transfer of data. When the selected tape unit is tested and is in an operational state, the status byte consisting of the CHANNEL END bit (bit 4) only will be presented to the channel.* The end status byte will include the CONTROL UNIT END bit (bit 2) if the Control Unit was addressed or an unusual condition was detected and caused the UNIT CHECK or UNIT EXCEPTION bit to be set while the Control Unit was busy independently of the Channel. The Control Unit is considered busy independently of the Channel during the interval between the acceptance of the status byte containing CHANNEL END and the acceptance of the status byte containing DEVICE END by the channel.*

The particular control operation is specified by the modifier bits (CCC) of the command. The description of each operation follows.

1.11 REWIND (CCC=000)

1.11.1 This command rewinds the tape on the selected unit to load point. If the tape is already rewound, the operation proceeds as in other CONTROL commands with respect to the presentation of the CHANNEL END and DEVICE END status bits. If the tape is not rewound, the CHANNEL END status byte will be presented at

*Exceptions to these statements are given under REWIND.

REWIND (CCC=000) (cont)

the completion of the operation in the Control Unit, i.e., once the rewind operation has successfully been initiated in the tape unit. Once the CHANNEL END bit has been accepted, the Control Unit is available.

1.11.2 The rewind operation terminates in the tape unit when the tape is positioned at load point and available for use. At this point a DEVICE END status byte is presented to the Channel indicating end of rewind. If the operation in the tape unit terminates unsuccessfully, e.g., due to power dropping, an end status byte will be presented containing the UNIT CHECK bit (Bit 6). CONTROL UNIT END is not returned in this case.

1.11.3 Since the CHANNEL END status byte on a successfully initiated rewind operation indicates that the operation is complete at the Control Unit level, unusual conditions or addressing of the Control Unit beyond this point will not result in the inclusion of the CONTROL UNIT END bit (Bit 2) in the end status byte.

1.12 REWIND WITH INTERLOCK (CCC=001)

1.12.1 This command rewinds the tape on the selected unit to the unload point and sets the interlock condition in the tape unit. The operation in the Control Unit terminates after the operation has been initiated in the tape unit. The end status byte consisting of the UNIT CHECK bit (Bit 6), the DEVICE END bit (Bit 5), and the CONTROL UNIT END bit (Bit 2) is presented to the channel. The operation in the tape unit terminates when the tape is positioned at the unload point.

1.12.2 If the unit set to the interlock condition is addressed (on other than a SENSE command), the status byte of that command will contain the UNIT CHECK bit (Bit 6) only, to indicate that the addressed tape unit is not ready. The interlock condition of the tape unit can only be removed by manual intervention.

1.13 ERASE (CCC=010)

1.13.1 The ERASE command moves the tape on the selected unit forward and erases tape for approximately 3.5 inches. The end status byte consisting of the DEVICE END bit (Bit 5) along with other bits, if any, will be presented to the channel when the erase timing in the Control Unit has expired. The tape is checked for spurious pulses arising from any portion of the tape that is unerased.

1.13.2 Performing an ERASE operation in the end-of-tape area causes an end status byte to be presented to the channel consisting of the UNIT EXCEPTION bit (Bit 7), the DEVICE END bit (Bit 5) and the CONTROL UNIT END bit (Bit 2).

1.14 WRITE TAPE MARK (CCC=011)

1.14.1 This command moves the tape on the selected unit forward generating an interblock gap of approximately 3.5 inches before writing the tape mark in the NRZI mode of operation. In the Phase Encoding mode the normal gap is generated before writing the tape mark burst. When writing a tape mark in 7-track NRZI mode, the parity mode setting is overridden (but not reset) and the tape mark is written with even parity.

WRITE TAPE MARK (CCC=011) (cont)

1.14.2 When the end-of-block is detected on Check Read, the end status byte, consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the channel. Performing this operation in the end-of-tape area results in the same end status byte as the ERASE operation.

1.15 BACKSPACE BLOCK (CCC=100)

1.15.1 This command moves the tape on the selected unit to the next interblock gap in the backward direction. When the end-of-block is detected on Read, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the channel.

1.15.2 Sensing a tape mark causes the UNIT EXCEPTION bit (bit 7) and the CONTROL UNIT END bit (bit 2) to be included in the end status byte along with the DEVICE END bit (bit 5).

1.15.3 During 7-track BACKSPACE BLOCK operations, tape marks may be erroneously identified with tapes generated by other than U6-C, U8-C, U12, U16, or other tape units which provide scatter correction of the LRC character. The verification of the tape mark is accomplished by reading forward.

1.16 BACKSPACE FILE (CCC=101)

1.16.1 This command moves the tape on the selected tape unit backward to the interblock gap beyond the next tape mark encountered. If a tape mark is not encountered, the tape will stop at load point. Sensing the tape mark does not set the UNIT EXCEPTION bit or the CONTROL UNIT END bit.

1.16.2 Erroneous termination of BACKSPACE FILE operations may occur when in 7-track mode due to uncertainty in detection of tape marks. This may occur during BACKSPACE FILE operations with tapes generated by other than U6-C, U8-C, U12, U16, or other tapes which provide scatter correction of the LRC character. Verification is obtained by reading forward. The BACKSPACE FILE operation terminates when the end-of-tape mark block is detected.

1.17 FORWARD SPACE BLOCK (CCC=110)

This command moves the tape on the selected unit to the next interblock gap in the forward direction. When the end-of-block is detected on Read, the end status byte consisting of the DEVICE END bit (bit 5) along with other bits, if any, will be presented to the channel. Sensing a tape mark is the same as in a BACKSPACE BLOCK operation.

1.18 FORWARD SPACE FILE (CCC=111)

This command moves the tape on the selected unit forward to the interblock gap, beyond the next tape mark encountered. Sensing the tape mark does not set the UNIT EXCEPTION bit or the CONTROL UNIT END bit.

The FORWARD SPACE FILE operation terminates when the end-of-tape mark block is detected.

1.20 MODE SET (DDMMM011)

1.20.1 The MODE SET command is used to select the data transfer mode of operation. Bits 0, 1, 2, 3, and 4 determine the mode selected. Once set, data transfer modes normally remain set until modified by another MODE SET command or reset by the channel. The reset conditions are 1600 bpi Phase Encoding mode (9-track), and 800 bpi NRZI mode (7-track). For the 7-track mode, the reset condition includes odd parity, data converter on, and translator off. If the data converter feature is not installed, the reset condition is odd parity, data converter off, and translator off. The 7-track and 9-track mode settings are independent of one another. The mode that prevails (7- or 9-track) will be the mode determined when the tape unit is selected on the next operation. The mode setting command (for 9-track operation), applies to a WRITE, WRITE TAPE MARK, or ERASE operation starting at load point. The setting holds for the tape unit until the tape is returned to load point and a new setting is received. The read operation requires no mode setting (for 9-track operation). The setting will be determined by reading the identification burst at the beginning of the tape. A burst of bits in the P track between load point and the first recorded tape block identifies a 1600 bpi tape, the lack of this burst identifies an 800 bpi tape. Again, this setting will be retained until the tape is returned to load point.

1.20.2 Seven-track operations require mode settings on write and read operations.

1.20.3 ALL MODE SET commands except REQUEST TIE are completed during the initial selection sequence. Normally CHANNEL END and DEVICE END are included in the status byte presented at the end of initial selection. When this status byte is accepted, the Control Unit is available for a new operation. For the REQUEST TIE command, the status presented at the end of initial selection is normally clear (binary zeros). After the single byte data transfer is complete, the status byte indicating termination will be presented to the channel. Normally the bits included are CHANNEL END and DEVICE END.

MODE SET commands will not clear the SENSE bytes when accepted.

1.20.4 MODE (000)

This defines a "NO OPERATION" command. No mode setting will be altered.

1.20.5 MODE (001)

This mode is used for failure-finding only. Non-diagnostic programs should not attempt to set this mode of operation.

1.20.6 MODE (010)

This mode defines a 7-track mode with odd parity, translator off, data converter on, and a density defined by the DD bits.

1.20.7 MODE (011)

When DD = 00, this mode defines a REQUEST TIE command. This operation causes a byte of information to be transferred to the Control Unit, to be used for error correction on 9-track NRZI tapes. If the following READ or READ BACKWARD operation is addressed to either a 9-track Phase Encoding only tape unit or a 7-track unit, data correction will not be attempted and the track-in-error information will be cleared.

When DD = 01, this mode defines a low gain setting for the next "read" or "space" operation. Low gain settings apply to operations on Phase Encoded or NRZI tapes. The low gain condition will be cleared at the end of the operation following the MODE SET.

1.20.8 MODE (100)

This mode defines a 7-track mode with even parity, translator off, data converter off, and a density defined by the DD bits.

1.20.9 MODE (101)

This mode defines a 7-track mode with even parity, translator on, data converter off, and a density defined by the DD bits.

1.20.10 MODE (110)

This mode defines a 7-track mode with odd parity, translator off, data converter off, and a density defined by the DD bits.

1.20.11 MODE (111)

This mode defines a 7-track mode with odd parity, translator on, data converter off, and a density defined by the DD bits.

1.30 MAINTENANCE COMMANDS

1.30.1 RESET FAILURE-FINDING MODES (00001011)

This command resets the Device Simulation Mode and Operation Monitor Mode, if they were set. The control unit will return to the normal state. The System Reset, or Selective Reset, will also reset these modes.

1.30.2 SET DEVICE SIMULATION MODE (01001011)

This command activates the tape unit simulation logic. The signals to the tape unit will be blocked and simulated return signals will be generated during the execution of subsequent commands. This facilitates the checkout of the control unit without a tape unit.

1.30.3 SET DEVICE SIMULATION MODE (01001011) (cont)

1.30.3.1 For write operation, the write data received from the Channel will be processed through the write logic, then will be fed back into the read recovery logic. The Cyclic Redundancy Check (CRC) frame will be generated, but a Longitudinal Redundancy Check (LRC) frame will not be generated. However, the content of the LRC register will be the LRC frame supposed to be written on the tape.

1.30.3.2 For read operation, the content of the CRC register will be used as the simulated data. The content will be shifted end-around one place from high to low order for every frame generated. The simulated data will be generated at nominal data frequency until it receives the data terminate signal from the Channel.

1.30.3.3 The output of CRC register will be added with the R.O. pattern (111010111) in binary addition before it is gated into the read recovery logic. The CRC register will be precleared only before a write, simulated write, or read operation.

To set up desired data in the CRC register for the simulated read, a write operation should be performed beforehand. The parity of the content of the CRC register depends on the number of characters written during the previous write operation. The vertical parity checker in the read recovery can be checked with the data having a wrong parity.

If the initial content or the shifted content of the CRC register does correspond with R.O. pattern, the generated data block will have a blank frame for every ninth frame. By this, the frame dropout checker in the read recovery can be checked.

1.30.3.5 For Write Tape Mark operation, the generated Tape Mark frame will be gated into the read recovery logic.

For space, or space file operation, one frame of the generated data from the CRC register will be gated into the read recovery logic. The tape mark indications will be set if the generated data correspond with the tape mark code.

1.30.3.6 The erase operation will be executed in the normal manner.

1.30.4 SET OPERATION MONITOR MODE (10001011)

This command activates the logic which transmits the Monitor Sense bytes instead of the Sense Data bytes during the subsequent sense operation(s).

The Monitor Sense bytes (5 bytes) provide detailed information about the operational condition caused by the last operation.

2. STATUS BYTE

2.1 The Status Byte provides the overall information about status and conditions detected in the operation completed. The Control Unit initiates the sequences to present status to the channel at the end of the Initial Selection Sequence, at the completion of unit selection of a CONTROL operation, and at the completion of the operation. The status bits are reset to binary zero when the status presented is accepted by the channel. The following defines the significance of binary one in each status bit.

	Bit Designation	Interpretation
2.2	0 ATTENTION	Indicates that a tape unit has become ready (i.e. Tape Unit Status A active and Tape Unit Status B inactive) after the Control Unit has detected a Non-Ready State in that tape unit. This status bit is indicative of an operator intervention at the tape unit (e.g. loading a new tape). This status is unsolicited and is not presented as a result of any previously initiated operation. The least significant four bits of the device address associated with the ATTENTION Status byte indicate the address of the tape unit which became ready. The monitoring of the state of each tape unit takes place when the Control Unit has completed the execution of previously issued commands. If either simultaneous feature is installed, both Control Units will attempt to present ATTENTION when required. Furthermore, when the Dual Access Control feature is installed, the ATTENTION bit will be presented to both I/O Interfaces. Changes of state on units not "existent" on an I/O Interface will not be presented to that interface.
2.3	1 STATUS MODIFIER	Present with the BUSY bit to indicate Control Unit busy. On a Control Unit with two I/O Channel Interfaces, Control Unit busy is indicated to one Interface if an Initial Selection Sequence is attempted while the Control Unit is presently operating with, or reserved by, the alternate I/O Interface.
2.4	2 CONTROL UNIT END	a. When the Control Unit completes a CONTROL operation that kept it busy independently of the channel, during which time it was either addressed (causing a Control Unit busy indication) or an unusual condition was detected (UNIT CHECK or UNIT EXCEPTION), CONTROL UNIT END will be presented with DEVICE END. The Control Unit is considered busy independently of the Channel during the interval between the acceptance of the CHANNEL END status byte and the DEVICE END status byte by the channel. b. Whenever a Control Unit busy sequence occurs on one I/O Interface of a Dual Access Control Unit, and the Control Unit is presently operating with, or reserved by, the alternate I/O Interface, a CONTROL UNIT END Status byte will be presented to the I/O Interface that received the Control Unit busy indication when the Control Unit completes the operation in progress, or is released by, the alternate I/O Interface.

	Bit Designation	Interpretation
2.5	2 CONTROL UNIT END	During the presentation of the Control Unit End Status byte to the I/O Interface that received the Control Unit busy indication, the alternate I/O Interface will not be denied access to the Control Unit.
2.6	3 BUSY	a. Present with STATUS MODIFIER to indicate Control Unit Busy. b. Present with status already stored if status pending for addressed tape unit, when the command is other than a TEST, SET INHIBIT STATUS or RESET INHIBIT STATUS.
2.7	4 CHANNEL END	For SENSE, REQUEST TIE, WRITE, READ and READ BACKWARD commands, CHANNEL END is presented with DEVICE END when the operation is completed at the Control Unit level. It is presented on CONTROL commands, after the tape unit is tested and available. On REWIND commands, when the tape is not initially at load point, CHANNEL END is presented at the completion of the operation at the Control Unit level. If early errors prevent tape motion, and the operation is aborted early, the CHANNEL END status bit is not sent to the channel. It is also presented at the end of initial selection with DEVICE END on MODE SET commands (except REQUEST TIE).
2.8	5 DEVICE END	a. Indicates that the operation (except a successfully initiated REWIND command) is complete at the Control Unit level. When errors are detected before tape motion is initiated, DEVICE END is not presented with error status. Operations involving data transfers that are aborted while in progress (e.g. due to Equipment Check) will cause DEVICE END to be sent with UNIT CHECK and CHANNEL END. b. Indicates that a REWIND has been completed at the tape unit level. If the REWIND terminates unsuccessfully in the tape unit, DEVICE END will be presented with UNIT CHECK.
2.9	6 UNIT CHECK	a. Indicates a bit in Sense Byte 0 has been set as a result of the current operation. (If the error condition is detected before tape motion is initiated, UNIT CHECK will be presented without end status.) b. The selected tape unit is busy, i.e., ready and rewinding or ready and under control of the other Control Unit. End status will not be presented with UNIT CHECK. When a rewinding tape unit is selected by the Control Unit which issued the rewind operation, the tape unit is busy until the DEVICE END status byte associated with the end of rewind has been accepted by the channel. c. A rewind operation terminated unsuccessfully in the tape unit. DEVICE END is presented with UNIT CHECK.

	Bit Designation	Interpretation
	6 UNIT CHECK (cont)	d. A READ BACKWARD, BACKSPACE BLOCK, or BACKSPACE FILE is attempted on a tape unit when the tape is positioned at load point. (No end status is presented in this case.) e. A REWIND WITH INTERLOCK has been completed at the Control Unit level, i.e. when the tape unit becomes non-ready. If the operation is initiated, DEVICE END will be presented with UNIT CHECK and CONTROL UNIT END.
2.10	7 UNIT EXCEPTION	Indicates: a. A WRITE, WRITE TAPE MARK, or ERASE operation is performed in the end-of-tape area. b. A tape mark is sensed during a READ, READ BACKWARD, FORWARD SPACE BLOCK, or BACKSPACE BLOCK operation. In cases a. and b. UNIT EXCEPTION is presented with DEVICE END (and CONTROL UNIT END on CONTROL operations).

3. Sense Data Bytes

3.1 The sense data provides detailed information about the unusual conditions detected in the last operation and the current status of the selected tape unit. Sense bits that set as a result of error or fault conditions during an operation will remain set until cleared upon initiation of a new command. Executing a SENSE command will not change the state of these bits (all those not marked with an asterisk). Bits that are marked with an asterisk (*) will reflect the current state of the selected tape unit. For example, if a "non-ready" condition is detected and the operation is aborted early, Tape Unit Status B and Intervention Required will set in sense bytes 1 and 0 respectively. If, between the time that the operation was aborted, and the SENSE command executed, the tape unit became "ready", then the sense data returned to the channel will be Intervention Required and Tape Unit Status A.

3.2 No additional sense information can be set as a result of executing a SENSE command once the command has been accepted (i.e. odd command byte parity and valid command code). The following tables describe the significance of the sense bytes.

SENSE BYTE 0		MODE OF OPERATION	
BIT	DESIGNATION	PHASE-ENCODING	NRZI
0	Command Reject	a. Set when a WRITE, WRITE TAPE MARK, or ERASE command was attempted on a file protected tape unit. b. Set when an invalid command is transmitted to the Control Unit. (This condition will not be set if a BUS OUT Check occurred on a command transfer.) c. The Tape Unit Incompatibility bit was set (Bit 7, Sense Byte 1).	Same
1	Intervention Required	Set whenever tape unit status A is inactive, i.e., a non-existent or non-ready tape unit was selected on other than a SENSE command. (Bit 1 is not set in Sense Byte 1.)	Same
2	BUS OUT Check	Set whenever even parity appears on the BUS OUT for data or command transfers. During WRITE operations, if this condition is set on a data transfer, the operation is terminated, and the error byte is not written on the tape. If the error occurs on the first data transfer Word Count Zero will be set in conjunction with BUS OUT Check.	Same If this condition is detected during the data transfer on a REQUEST TIE command, the operation terminates but the information received is ignored. Any TIE information already stored is not disturbed.
3	Equipment Check	Set whenever an Equipment Check occurs, i.e., bits 0, 1, or 5 of Sense Byte 4 have been set.	Same
4	Data Check	Set whenever a Data Check occurs, i.e., bit 0 of Sense Byte 1, or bits 0, 1, 2, 3, 4 of Sense Byte 3 have been set.	Same

SENSE BYTE 0 (cont) — MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
5	Overrun	Set if service is requested on the I/O Interface but data cannot be transferred due to a late response signal from the channel. If this occurs on the first data transfer of a **WRITE** operation, Word Count Zero will be set in conjunction with Overrun. (Not set on REQUEST TIE or SENSE commands.)	Same
6	Word Count Zero	a. Set during a WRITE operation if transfer of data is prevented when the first byte of data is requested. This can be due to a "COMMAND OUT" response to the data byte request, even parity detected for the data byte transfer (see BUS OUT Check), or a channel overload (see Overrun). No new tape motion will occur if any of these conditions are detected. If non-stop operation is indicated, the previous operation will terminate properly. b. Set if the end-of-block is detected on READ or READ BACKWARD operations before any data bytes are recognized (missed start sentinel).	Same
7	Data Converter Check	Not applicable—always set to zero.	Set on 7-track operations only.

SENSE BYTE 1

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
0	Noise	When Reading or Read Checking data from Phase Encoded tapes, the checks performed to set the Noise bit are essentially the same as in NRZI recording. However, two basic differences pertaining to the quality of the check exist. First, when checking for tape hash, the outputs of the block detector circuits for each track are monitored. Since these circuits tend to reject noise, a single "bit pick-up" would not activate the block detector outputs and the Noise bit would not set. In NRZI recording, the Noise bit would set, since the data lines are monitored directly. Second, when checking for gaps in the data, or data "drop-outs", all block detector outputs must be deactivated together, before the Noise bit sets. In Phase Encoded recording, a signal results from writing either a "1" bit or a "0" bit. Therefore, within the block, a signal is normally present in all tracks. Thus only a relatively serious condition could cause the Noise bit to set (e.g., a lateral crease in the tape). In NRZI recording, however, a signal is present only when "1" bits are written. Therefore, a small defect in one track, when recording one bits only in that track, will cause the Noise bit to set. The Noise bit, then, should set relatively infrequently, as compared to the NRZI mode of operation.	a. Tape Hash During WRITE or WRITE TAPE MARK operations, data (or noise due to tape defects) was detected on Read Check sooner than was expected. During ERASE operations, data (or noise due to tape defects) was detected on Read Check while the tape was being erased. b. During WRITE or WRITE TAPE MARK operations, while Read Checking the recorded data, a gap in the data was detected which was not long enough to set the end-of-block condition. This can occur due to unrecordable areas on the tape. c. During READ, READ BACKWARD, FORWARD SPACE BLOCK, and BACKSPACE BLOCK operations a data "drop-out" occurred on Read which was not long enough for the end-of-block condition to be detected. For conditions a, b, and c, above tape motion does not cease in the middle of the block. Writing (or erasing) will continue to the normal termination point. d. Bit 6 of Sense Byte 4 was set (Tape Fault).

SENSE BYTE 1 (cont)

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
1*	Tape Unit Status A	Selected and Ready	Same
2*	Tape Unit Status B	Not ready, rewinding, or under control of the other Control Unit.	Same

Status A	Status B	Tape Unit Status	Bit Set in Status Byte
0	0	Non-existent	UNIT CHECK
0	1	Not Ready	UNIT CHECK
1	0	Ready and not busy	———
1	1	Ready and busy, i.e. rewinding or under control of other Control Unit.	UNIT CHECK

3*	Seven Track	Same	The selected unit has a seven-track head installed.
4*	Load Point	The tape on the selected unit is positioned at load point.	Same
5*	End of Tape	The tape on the selected unit is in the end-of-tape area.	Same
6*	File Protect	The tape on the selected unit does not have a write enable ring.	Same

SENSE BYTE 1 (cont)

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
7	Tape Unit Incompatibility	a. Tape Unit is selected on any command requiring tape motion and any of the following conditions occur: Addressed tape unit is a U6-C or U8-C, 7- or 9-track, and is indicating the phase encoding mode of operation. Addressed tape unit is a U12 or U16, 7-track, and is indicating the phase encoding mode of operation. Addressed tape unit is a U12 or U16, 9-track, and failed to reset to 1600 bpi mode. (Load point only.)	Same
		b. Tape unit is selected for a "write-type" operation from load point and the following occurs: Addressed tape unit is U6-C or U8-C, 9-track type.	b. Tape unit is selected for a "write-type" operation from load point and the following occurs: Addressed tape unit is a U12 or U16, 9-track, and failed to set to 800 bpi mode.
		c. Tape unit is selected for a "read-type" operation from load point and any of the following conditions occur: Addressed tape unit is a U6-C or U8-C, 9-track, and the tape is written in 1600 bpi phase encoding mode. Addressed tape unit is a U12 or U16, 9-track, and failed to set 800 bpi mode when the tape is written in 800 bpi NRZI mode.	Same
		d. A "write-type" operation was attempted on a Uniservo 12, 6-C, or 8-C on the Second Control Unit (CUB).	Same

NOTE: In cases a, b, and d above, no tape motion occurs as a result of the attempted operation.

In case c above, the condition is detected after the the first "read type" operation has been initiated. If the "read-type" command is to be attempted a second time, a REWIND command should first be executed in order to reposition the tape. Case d. does not apply if Bank Write/Write Simultaneity Feature is installed (F1105-00).

SENSE BYTE 2

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
0	Track in Error	Not applicable—Always set to zeros.	This sense byte contains the track-in-error indicator bits that are set at the end of a READ or READ BACKWARD operation if a Data Check has been encountered. A single 1 bit in any bit position indicates a single-track error, the bit position indicates the track in error. Binary zeros in bits 0 → 7 implies bit P. If bits 6 and 7 contain binary ones, then a multiple track error has been encountered and no track error identification has been made. At the completion of a properly executed READ or READ BACKWARD operation with no Data Check, sense byte 2 contains at least bits 6 and 7 set to 1's. No error correction is attempted when operating with seven-track tape units. Bits 6 and 7 are set to 1's in sense byte 2.
7			

SENSE BYTE 3

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
0	R/W VRC	A Vertical Redundancy Check occurred on a data frame without a Dead Track indication during a WRITE, READ, or READ BACKWARD operation (Uncorrectable error).	a. A Vertical Redundancy Check occurred on a data frame or CRC frame during a READ or READ BACKWARD operation. This indicator is not set after an Overrun indication. b. A speed check error occurred during a WRITE or WRITE TAPE MARK operation.
1	Multiple Dead Track Check-Track Start failure/LRC	a. A marginal signal occurred in more than one track on a READ or READ BACKWARD operation. (Uncorrectable.) b. Valid information was not detected in at least one track while Read Checking the preamble during a WRITE operation. This indicates a track start failure, possibly indicating the track was never written on the tape. This check is only performed during the preamble before the circuits that detect marginal signals are operable. Normally Bit 4 of Sense Byte 3 will set in conjunction with this bit if the track is missing entirely.	A longitudinal Redundancy Check occurred during a WRITE, WRITE TAPE MARK, READ, or READ BACKWARD operation.
2	Skew	Excessive skew is detected during a WRITE, READ or READ BACKWARD operation. (Deskew register underflow.)	Excessive skew detected while read checking recorded data on a WRITE or WRITE TAPE MARK operation.
3	Postamble Check/CRC	Set when the postamble following the data is not read correctly, or is recognized before the actual end of data (early stop sentinel).	A Cyclic Redundancy Check occurred during a READ or READ BACKWARD operation (9-track only).

SENSE BYTE 3 (cont)

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
4	Dead Track Check/W VRC	a. Indicates at least one track with marginal signal during WRITE or WRITE TAPE MARK operations. b. Indicates a marginal signal in only one track during a READ or READ BACKWARD operation (correctable error). This bit will not be set if a multiple track error occurs (see Bit 1). If I = 1 in the read command code, and this bit is set, Data Check will set. However, if this bit is set and I = 0 in the read command code, Data Check will not set. In either case, the data is correct. c. Indicates that a tape mark was not properly detected on the Read Check of a WRITE TAPE MARK operation.	A Vertical Redundancy Check occurred on a data frame or CRC frame during a WRITE or WRITE TAPE MARK operation.
5*	Tape Unit—1600 bpi	The selected tape unit is set to 1600 bpi mode.	Same — This bit is always set to zero when selecting a 7-track tape unit.
6*	Backward	The selected tape unit is conditioned for backward tape motion.	Same
7		NOT USED — Always set to zero.	Same

SENSE BYTE 4

MODE OF OPERATION (cont)

BIT	DESIGNATION	PHASE-ENCODING	NRZI
0	Runaway Check	a. While read checking recorded data during WRITE, or WRITE TAPE MARK operations, the end-of-block was not detected within at least 8.3 ms (U12 or U6-C) or 2.9 ms (U16 or U8-C) after writing has ceased. b. During all read-type operations, if data is not detected within at least 7.0 seconds (U12 or U6-C) or 2.5 seconds (U16 or U8-C).	Same
1	Tape Motion Fault	a. Tape unit failed to respond to a "start" command. Tape motion may or may not have occurred. b. Tape motion stopped independently of the Control Unit during an operation requiring tape movement. (This condition will be detected if a backward operation is executed into load point.)	Same
2 ↓ 4	These bits are reserved for failure finding mode.		
5	Stall	Indicates that the Control Unit is hung up for more than 2.5 seconds.	Same
6	Tape Fault	During WRITE or WRITE TAPE MARK operations, indicates that the end-of-block was detected sooner than expected. False end-of-block can occur if a data dropout (all tracks) is longer than 790 μs. on a U12 or U6-C, or more than 280 μs. on a U16 or U8-C.	Same
7	This bit is reserved for failure-finding mode.		

4. MONITOR SENSE BYTES

	BYTE Ø	BYTE 1	BYTE 2	BYTE 3	BYTE 4
BIT POS.	PC1M	PC2M	PC3M	PC4M	PC5M
0	MPC00	PFW	PRERR	DT1 CY1	PZER0 L0
1	MPC01	PFR	SENT	DT2 CY2	PZER1 L1
2	MPC02	PFB	TMD	DT3 CY3	PZER2 L2
3	6AV	PFSFL	PSTAT	DT4 CY4	PZER3 L3
4	7AV	PFFL	CHTRM	DT5 CY5	PZER4 L4
5	8AV	PFRW	PHASE	DT6 CY6	PZER5 L5
6	RES	PFWTM	DTP CYP	DT7 CY7	PZER6 L6
7	SIM	PFERS	DTO CY0	PZERP LP	PZER7 L7

MONITOR SENSE BYTE DESCRIPTION

4.1 PC1M

4.1.1 MPC00, MPC01, MPC02 - Contents of CU Program Counter, useful when the SB45 (Stall Condition) FF is set during the execution of any command other than Mode Set Commands. These 3 FF's will then indicate the CU cycle which was effective when the Stall Condition occurred.

4.1.2 6AV, 7AV, 8AV - Status Lines from Servo presently being addressed.

6AV	7AV	8AV		
1	0	0	U6-C	Servo Available
1	1	0	U12	
0	0	1	U8-C	
0	1	1	U16	

Any combination other than those listed will result in an unavailable servo.

4.1.3 RES (Reserved) - Indicates that the CU is available for use by only one channel.

4.1.4 SIM - Simulator Mode of Operation in effect.

4.2 PC2M

These bit positions indicate the previous non-Sense, non-Mode Set Command (except Request Tie) executed by the Control Unit.

PFW - Previous Function Write

PFR - Previous Function Read (Forward or Backward)

PFB - Previous Function Backward

PFSFL - Previous Function Space (Forward or Backward)

PFFL - Previous Function File

PFRW - Previous Function Rewind

PFWTM - Previous Function Write Tape Mark

PFERS - Previous Function Erase

All zero bits in PC2M represent the generally cleared condition of the CU or a previously executed Request Track in Error Command.

4.3 PC3M

PRERR - Program Error. Attempted backward operation (Read Backward or Space Backward) with servo at Load Point.

SENT - Ending Sentinel of the Postamble of a phase recorded data block detected on the previously executed Read type operation.

TMD - Tape Mark Detected.

PSTAT - Inhibit Status FF set in Channel Interface Package.

CHTRM - Channel Termination ($\overline{\text{TERM}}$) received by the Control Unit on Read (forward or backward) operations before entire block of tape data transferred.

PHASE - Phase Mode (1600 ppi) set.

4.4 PC4M-PC5M - The remaining two bits of Monitor Sense Byte three and Monitor Sense Bytes four and five are dual indications dependent upon the type of servo setting (Bits 5 of Normal Sense Byte 3 ($\overline{\text{NRZ}}$). NRZ active (high for a phase recording servo) will cause the contents of the Dead Track Register (DTP, 0-7) and the Zeros Alert Register (PZERP, 0-7) to be transmitted to the Channel.

DTP-DT7
CYP-CY7
PZERP-PZER7
LP-L7

NRZ active (high when servo recording in non-return-to-zero mode) will cause the contents of the Cyclical Redundancy Register (CYP, 0-7) and the Longitudinal Parity Check Register (LP, 0-7) to be transmitted to the channel.

DISC FILE CONTROL

TYPE 5024

1. COMMAND REPERTOIRE:

The table below summarizes all the commands executable by the subsystems. The M bit, when zero defines normal operation. When one, operation is in the multiple track mode.

1.1 TABLE OF VALID COMMAND CODES WITH AND WITHOUT M/T

TYPE	COMMAND	BINARY CODE 0 1 2 3	BINARY CODE 4 5 6 7	HEX CODE SINGLE-TRK	HEX CODE MULTI-TRK
CONTROL	NO OPERATION	0 0 0 0	0 0 1 1	03	
	SEEK	0 0 0 0	0 1 1 1	07	
	SEEK CYLINDER	0 0 0 0	1 0 1 1	0B	
	SPACE COUNT	0 0 0 0	1 1 1 1	0F	
	RECALIBRATE	0 0 0 1	0 0 1 1	13	
	SEEK HEAD	0 0 0 1	1 0 1 1	1B	
	SET FILE MASK	0 0 0 1	1 1 1 1	1F	
READ	READ IPL (4)	M 0 0 0	0 0 1 0	02	82
	READ DATA	M 0 0 0	0 1 1 0	06	86
	READ KEY-DATA	M 0 0 0	1 1 1 0	0E	8E
	READ COUNT	M 0 0 1	0 0 1 0	12	92
	READ RO	M 0 0 1	0 1 1 0	16	96
	READ HOME ADDRESS	M 0 0 1	1 0 1 0	1A	9A
	READ COUNT, KEY, DATA	M 0 0 1	1 1 1 0	1E	9E
WRITE	WRITE SPECIAL COUNT, KEY, DATA (1)	0 0 0 0	0 0 0 1	01	
	WRITE DATA	0 0 0 0	0 1 0 1	05	
	WRITE KEY-DATA	0 0 0 0	1 1 0 1	0D	
	ERASE	0 0 0 1	0 0 0 1	11	
	WRITE RO	0 0 0 1	0 1 0 1	15	
	WRITE HOME ADDRESS	0 0 0 1	1 0 0 1	19	
	WRITE COUNT, KEY, DATA	0 0 0 1	1 1 0 1	1D	
SEARCH	SEARCH EQUAL ID	M 0 1 1	0 0 0 1	31	B1
	SEARCH HIGH ID	M 1 0 1	0 0 0 1	51	D1
	SEARCH HIGH OR EQUAL ID	M 1 1 1	0 0 0 1	71	F1
	SEARCH EQUAL KEY	M 0 1 0	1 0 0 1	29	A9
	SEARCH HIGH KEY	M 1 0 0	1 0 0 1	49	C9
	SEARCH HIGH EQUAL KEY	M 1 1 0	1 0 0 1	69	E9
	SEARCH EQUAL HOME ADDRESS	M 0 1 1	1 0 0 1	39	B9
	SEARCH EQUAL KEY DATA (2)	M 0 1 0	1 1 0 1	2D	AD
	SEARCH HIGH KEY DATA (2)	M 1 0 0	1 1 0 1	4D	CD
	SEARCH HIGH EQUAL KEY DATA (2)	M 1 1 0	1 1 0 1	6D	ED

COMMAND REPERTOIRE (continued)

Table of Valid Command Codes with and without M/T (continued)

TYPE	COMMAND	BINARY CODE 0 1 2 3	BINARY CODE 4 5 6 7	HEX CODE SINGLE-TRK	HEX CODE MULTI-TRK
SEARCH (cont)	CONTINUE SCAN EQUAL (3)	M 0 1 0	0 1 0 1	25	A5
	CONTINUE SCAN HIGH (3)	M 1 0 0	0 1 0 1	45	C5
	CONTINUE SCAN HIGH EQUAL (3)	M 1 1 0	0 1 0 1	65	E5
	CONTINUE SCAN NO COMP (3)	M 1 0 1	0 1 0 1	55	D5
	CONTINUE SCAN SET COMP (3)	M 0 1 1	0 1 0 1	35	B5
	CONTINUE SCAN SET COMP (3)	M 1 1 1	0 1 0 1	75	F5
SENSE	TEST I-O	0 0 0 0	0 0 0 0	00	
	SENSE I-O	0 0 0 0	0 1 0 0	04	
	SENSE RESERVE	1 1 1 1	0 1 0 0	F4	
	SENSE RELEASE	1 1 0 1	0 1 0 0	D4	

NOTE:
1. INVALID IF NO RECORD OVERFLOW FEATURE
2. INVALID IF NO FILE SCAN FEATURE
3. INVALID IF NO RECORD OVERFLOW AND FILE SCAN FEATURES
4. THE M BIT WILL BE IGNORED BY THE CONTROL UNIT ON INITIAL LOAD AND A SINGLE RECORD WILL BE READ.

1.2 Set File Mask (0001 1111)

1.2.1 Most commands to the control unit will be part of a "command chain." The Set File Mask command affects certain subsequent commands in the chain. Although the Set File Mask can be executed anywhere in the chain, issuance of this command as the first command protects the entire chain. If an attempt is made to issue more than one Set File Mask within a chain, a Unit Check status, associated with Command Reject sense information will result.

1.2.2 Execution of this command causes one byte of data, called a Mask Byte, to be transmitted from the channel to the control unit. The status pair Device End and Channel End signal completion of the command.

1.2.3 The effect of the Mask Byte on Write Commands is as follows:

Mask Byte	Writes Permitted
00XYYXXX	All except Home Address and TD Record
01XYYXXX	None
10XYYXXX	Data or Key and Data
11XYYXXX	All

Mask Byte	Seeks Permitted
YYX00XXX	All
YYX01XXX	Head and Cylinder
YYX10XXX	Head
YYX11XXX	None

COMMAND REPERTOIRE (continued)

Set File Mask (0001 1111) (continued)

1.2.4 The File Mask is cleared to all zeros under the following conditions:

1. End of command chain.
2. Control unit is master cleared.
3. Channel indicates Selective Reset.
4. Channel indicates System Reset.

1.3 Seek Commands

1.3.1 The Seek Commands cause the transfer of six bytes of addressing information to the control unit. Only two of the six bytes are actually used; the remaining bytes are provided for possible future expansion of capabilities.

1.3.2 The significance of the bytes is listed below. The range is the decimal equivalent of the binary number range possible.

Byte	Function	Inclusive Range
0	Not used	Must be zero
1	Not used	Must be zero
2	Not used	Must be zero
3	Cylinder address	0-202
4	Not used	Must be zero
5	Head address	0-9

1.3.3 The Seek command allows positioning to any track and the selection of any Head in order to specify which of the Dics surfaces is to be used. Only Bytes 3 and 5 of the Address are significant when addressing the 8411 Disc.

The Seek Cylinder command is identical to the Seek command when used in addressing the 8411 Disc.

The Seek Head command allows the selection of any Head. Byte 3 of the address is ignored so that no physical positioning motion will occur.

1.3.4 Channel End status will be presented to the Channel after the transfer of the six address bytes to the Control Unit.

Device End status will be presented with Channel End in the case of the Seek Head.

Device End status will not be presented until the completion of Motion Control in the cases of the other Seeks.

1.3.5 By issuing a Seek command to one device and another command to a second device, it is possible to overlap the two commands. Seek commands to all eight devices can be overlapped in this fashion.

COMMAND REPERTOIRE (continued)

1.4 Write Commands

Write commands cause information to be transferred from the channel and stored on the disc. The control unit will automatically generate and append the appropriate Cyclic Check bytes to the record. There are two classes of Write commands; Format Writes and Data Writes. The Format Write commands are used to initialize the recording area; whereas the Data Write commands are the commands used by the ultimate user of the records.

1.4.1 Format Write Commands

After each command is completed, Channel End and DeviceEnd status are presented to the channel and the control unit continues to erase the track operated on. Device End will cause chaining in the channel and subsequent commands in the chain will be received and executed by the subsystem. After the last command in the chain has been responded to by Channel End and Device End, the control unit continues to erase the track until the Index Mark is reached. Note that Device End does not signal the ultimate end of a command as it does on more typical 9000 series subsystems. If the Control Unit should be addressed after Channel End and Device End status have been presented but before the Index Mark is reached, Busy status will be presented to the Channel When the operation is complete, Control Unit End status will be presented.

1.4.1.1 Write Home Address (0001 1001)

This command causes the Home Address area to be written. The channel must send five bytes of information to the subsystem:

Flag byte (one byte)
Cylinder No. (two bytes)
Head No. (two bytes)

1.4.1.2 Write Track Descriptor Record (0001 0101)

This command causes the TD Record to be written. This record is unique, from the hardware standpoint, in that it is the first record following the Home Address and it is not preceded by an Address Marker.

The Flag Byte and all check bytes are provided by the control unit. The remaining bytes (eight in the Count Area plus Key Area information plus Data Area information) must be provided by the channel. If the channel provides less bytes than are needed, the control unit writes binary zeros so that the Key and Data Areas conform to the lengths specified in the Count Area. However, because R_0 is intended to specify alternate tracks, R_0 will normally have no key Area.

This command must be chained from a Write Home Address, or a Search HA that was equal on all five bytes of the Home Address.

COMMAND REPERTOIRE (continued)

1.4.1.3 Write Count, Key and Data (0001 1101)

This command causes records similar to Data Record R_1, to be written. The control unit provides the Address Marker, the Flag Byte, and the necessary Cyclic Check bytes. The Remaining bytes must be supplied by the channel. If the channel provides less bytes than are needed, the control unit pads binary zeros so that the Key and Data Areas conform to the lengths specified in the Count Area.

This command should be chained from a Write TD Record, another Write Count, Key and Data, a Search Equal ID, or Search Equal Key command.

Write Special Count, Key, and Data (0000 0001). See Section on Overflow Records for details.

1.4.2 Data Write Commands

1.4.2.1 Write Data (0000 0101)

This command causes data to be obtained from the channel by the control unit and recorded in the Data Area. The length is specified by the Length Byte in the previously recorded Count Area. If the channel does not provide enough data to allow the actual data length to conform to the Data Length byte; the control unit pads the binary zeros necessary to attain conformity.

This command should be chained from a Search Equal ID, or from a Search Equal Key command.

1.4.2.2 Write Key and Data (0000 1101)

This command causes information to be obtained from the channel and recorded in the Key and Data Areas of the record. The lengths are specified by the three Length Bytes in the previously recorded Count Area. If the channel does not provide enough data to allow the actual lengths to conform to the Key and Data Length bytes; the control unit pads binary zeros, as necessary, to attain conformity.

This command should be chained from a Search Equal ID command.

COMMAND REPERTOIRE (continued)

1.5 Search Commands

On search operations, the channel operates in a write mode while the device operates in a read mode. These two sources of information are compared by the control unit. The comparison made is device to channel. Thus a 2_{16} on the disc compared with a 1_{16} at the channel meets the criterion for a "find" on a Search High command.

The information processed by the control unit is error checked as the search is executed.

If the find is made (and no errors occur) the status bits sent to the channel are: Status Modifier, Channel End, and Device End. (If the Unit Check bit is set, Status Modifier will not be set). If a find is not made, the status bits are: Channel End, and Device End. The presence or absence of Status Modifier thus controls branching within the command chain.

1.5.1 Multiple Track Operation

On all search commands, the "M" (multiple track) bit allows operation within cylinder, rather than head boundaries. If M is zero, head switching does not take place. If M is one, the "Head Register" is incremented by one when the Index Marker is detected. If Head switching has occurred and the search command is repeated; the search will continue on the next head.

The M bit should be set to one with discretion. For example, if M is a one and the Index Marker is detected before an entire track has been searched, the first portion of the first track will be ignored on the search.

Head switching will continue to occur until End-of-Cylinder is detected.

1.5.2 Search Home Address Equal (M011 1001)

This command causes two bytes of Cylinder Number and two bytes of Head Number from the disc to be compared with four bytes of information from the channel. The Flag Byte is not transferred or compared during this command. The comparison made is bit by bit binary. An equal condition is indicated by the presence of the Status Modifier bit in the Status Byte.

1.5.3 Search Identifier Equal (M011 0001)

The term "Identifier" (ID) is introduced to define the five bytes of Cylinder, Head, and Record Number bytes located in the Count Area. The ID to be compared is the ID following the next Address Marker or Index Marker. In the latter case, the comparison is on the TD Record.

COMMAND REPERTOIRE (continued)

1.5.4 Search ID High (M101 0001)

This command is similar to the Search ID Equal command except that a find results when the ID on the disc is greater than the information presented by the channel.

1.5.5 Search ID Equal or High (M111 0001)

This command is similar to the other two Search ID commands except that a find is made if the comparison indicates either equal or high.

1.5.6 Search Key

The Search Key commands cause information from the Key Area of the disc to be compared to information from the channel. The key on which comparison is made is:

1. The Key Area of the record following the next Address Marker or;
2. The Key Area of the TD Record, if chaining is from a Search ID that compared on the ID of the TD Record.

The Search Key commands never return a Status Modifier bit if the Key Length of the record examined is zero.

1.5.7 Search Key and Data (these Search commands are associated with the File Scan Feature, F1099-00).

These search commands cause a comparison of both the Key and Data Areas of a record. It is possible to selectively compare any byte(s) in these two areas. The "Inhibit Byte" (a byte of all binary ones) makes the selective comparison possible. If an Inhibit Byte appears in the information coming from the channel (but not the disc); then comparison is not made on the byte coming from the disc that was destined to be compared with the channel byte. By making the first n channel bytes all binary ones (where n is the number of bytes in the Key Area) these search commands can effectively be reduced to "search data." There are no restrictions on the number or placement of Inhibit Bytes. These search commands may be used on records where the Key Area field is nonexistent.

Note that reading of a record, once found, will typically require an additional revolution of the disc.

COMMAND REPERTOIRE (continued)

1.6 Read Commands

On all read commands, the control unit reads information from the discs, checks information for errors, strips off the Cyclic Check bytes, and presents the information to the channel.

On all read commands, the M bit allows operation within cylinder, rather than head, boundaries. If M is zero, head switching does not take place. If M is one, the Head Register is incremented by one when the Index Marker is detected. If head switching has occurred, and the read command is repeated; the read will continue on the next head.

Since the TD Record is not preceded by an Address Marker, it cannot be read by this command.

1.6.1 Initial Program Load (M000 0010)

1.6.1.1 Facilities will exist in the central processor to select one device as a source of information for initial loading of a program. Additionally, a switch will exist which will transmit a command code of 0000 0010 to that selected device. The entire system should be "reset" before the IPL command is executed. The M Bit will be ignored and a single record will be read.

1.6.1.2 When this subsystem receives the IPL command, it will:

1. Cause the selected device to move to head zero, cylinder zero.
2. Wait for Index Marker.
3. Skip the following Home Address and TD Record.
4. Present the data portion of record one to the channel. Error checks are similar to those provided for Read Data commands.
5. At the end of record one, Channel End and Device End are presented to the channel.

1.6.2 Overflow Records (Provided by Feature F1098-00)

1.6.2.1 Provisions exist in the control unit so that record lengths can be limited by the cylinder, rather than the head, boundaries.

A portion of an overflow record which is written on one track is called a record segment. The Write Special Count, Key, and Data (0000 0001) command is provided for formatting all segments of an overflow record except the last. The Write Special Count, Key and Data differs from a Write Count, Key, and Data (0001 1101) only in that a one bit is written in bit position one of the Flag Byte.

COMMAND REPERTOIRE (continued)

1.6.2.2 All overflow segments must:

1. Be recorded as the first record following the TD Record except the 1st segment.
2. Not be on a defective track.
3. Not be on an alternate track.
4. Be full track records except the last segment.

The Count Areas in a record pertain to the segment of the record on that track, rather than the aggregate record.

1.6.2.3 A one bit in bit position one of the Flag Byte alters the operation of the following commands:

Read Data
Read Key and Data
Read Count, Key, and Data
Write Data
Write Key and Data

1.6.2.4 After completing the read or write operation on the first segment, the control unit waits for the Index Marker. When the Index Marker is reached, the control unit selects the next sequential head and searches for the first Address Marker on the track. It then processes the Data Area of this segment. The operation continues until a record segment is detected which contains a zero bit in Flag Byte bit position one. At the end of data transfers involving this segment, the operation is terminated.

Operations need not start on the first segment of an overflow record. The first segment to be entered is processed as though it were the first segment.

1.7 Miscellaneous Commands

The following commands cannot be categorized as Seek, Write, Search, Read or Sense. No information other than the command itself is transferred on the I-O channel on any of the commands.

1.7.1 Recalibrate (0001 0011)

The device determines the accessor movement to attain a new cylinder position on the basis of the present accessor position, rather than from a fixed reference. Consequently, it is possible for the accessor to "get lost" after a period of operation; perhaps because of electrical noise. The Recalibrate command is provided to give the device a new absolete reference position to allow continued operation if this situation should arise.

This command causes the device to seek head zero and cylinder zero. Channel End is generated as soon as the positioning information has been forwarded to the device, Device End on completion of Motion Control. This command operates under the constraints imposed by the "seek portion" of the File Mask.

COMMAND REPERTOIRE (continued)

1.7.2 No Operation (0000 0011)

This command causes the control unit to respond with Channel End and Device End. The addressed device takes no action.

1.7.3 Space Count (0000 1111)

This command enables the control unit to pass over an unreadable Count Area to gain access to subsequent good records. This command causes the control unit to search for the next Address Marker; when detected, Channel End and Device End are presented to the channel.

1.7.4 Erase (0001 0001)

This command is used to erase to the end of a track after a Track Overrun has occurred. The command causes the track to be erased from the end of the Data Area of the record on which the preceding search was satisfied; or the record just written by Write Count, Key, and Data; to the end of the track. Channel End and Device End are generated when the Index Mark is reached.

1.7.5 Test I-O (0000 0000)

This command allows the program to interrogate the Status Byte stored in the control unit while inhibiting status from other control units on the same I-O channel. Receipt of this command will cause the control unit to transmit the content of the eight-bit Status Register (the "register" may be hypothetical in the case of some bits) to the computer. Then, any control logic that would tend to send a Status Byte to the channel will be cleared. The Status Register itself will remain set to allow meaningful observation of the control unit's maintenance panel. The net effect of the command is to report and then clear impending interrupt conditions.

The Test I-O command does not have a status per se, the Status Byte transferred is the result of a previous command.

1.7.6 Selective Reset and System Reset

These are not commands in the usual sense. The effect produced by either of these conditions is identically the same as if the Master Clear switch on the maintenance panel of the control unit were depressed; all memory elements in the control unit are reset. No status is presented as a result of a Reset.

Any command in progress when the Reset condition was detected is stopped immediately and any information received by the channel as a result of the command should be regarded as invalid.

COMMAND REPERTOIRE (continued)

1.8 Sense Commands

1.8.1 When the Unit Check bit in the Status Byte is a one, additional details on the nature of the unusual condition are available in the form of "Sense Bytes". The Sense I-O commands present these bytes, in sequential order, to the channel; the channel may accept as many of the 32 possible bytes as it wishes.

1.8.2 There are three types of Sense I-O commands. The basic command merely causes Sense Bytes to be presented to the interface.

The other two Sense I-O commands are associated with the Dual Access Control Unit Feature. A Sense Reserve command from an I-O channel reserves use of the subsystem for the exclusive use of this channel until a Sense Release command is received at the subsystem. During the time interval between receipt of Sense Reserve and receipt of Sense Release, the alternate channel will receive a "Busy Status" in response to commands. All three Sense commands present Channel End and Device End status upon completion of the command.

The first 6 sense bytes are for the normal error recovery and the remaining 8 sense bytes are for on-line diagnostic and failure finding procedures. The transfer may be limited to the first 6 bytes if the CCW byte count is set to 6 and the incorrect length indicator suppressed.

1.8.3 SENSE bytes, except sense byte 3, indicate conditions which occurred in the control unit and selected device during the previous operation. Snese byte 3 indicates the present device status.

Sense data transfer rate is the same as the read or write data transfer rate.

SENSE bytes 0, 1, 2, and 5 are reset to all zeros during the early part of the initial selection sequence for commands other than TEST I-O and SENSE, if no status is stacked on selected device.

SENSE commands present all zero status at the end of the initial selection sequence even if the selected device is not operable.

1.8.4 SENSE I-O

1.8.4.1 SENSE I-O performs the operations described above.

COMMAND REPERTOIRE (continued)

1.8.4.2 SENSE RESERVE

The Sense Reserve command includes all of the functions of the Sense I-O command, and in addition, causes the control unit to become reserved to the channel issuing the command.

Once the control unit becomes reserved to a channel, it remains reserved until that channel releases the control unit by issuing a Sense Release command or a system reset is performed.

If a Set File Mask command precedes the Sense Reserve command in the same command chain, the Sense Reserve is rejected with Unit Check (Command Reject and Invalid Sequence).

1.8.4.3 SENSE RELEASE

The Sense Release command includes all of the functions of the Sense I-O command, and in addition, causes the reservation of the control unit to be terminated.

If a Set File Mask command precedes the Sense Release command in the same command chain, the Sense Release command is rejected with Unit Check (Command Reject and Invalid Sequence).

2. STATUS BYTE

2.1 Two Status Bytes will typically be presented to the channel during the execution of one command. The first byte (typically all zeros), will be transmitted before data services are requested. The second byte will be transmitted after all data have been operated on and the results checked for validity. No means of suppressing status, other than that required by SU00039 will be provided.

The table below lists the significance of one bits in the Status Byte.

	Bit Position	Description	Interpretation
2.2	0	Attention	Set when power is brought up on attached device.
2.3	1	Status Modifier	1. A search command has been executed and the condition called for by the command has been met. 2. Modifies the Busy status to indicate that the control unit, rather than the device, is busy.
2.4	2	Control Unit End	1. This is, in a sense, an unsolicited status. If an I-O channel requests service and the control unit responds with a Busy Status; then at the next non-busy opportunity, a Control Unit End Status is presented to that same requesting I-O channel.
2.5	3	Busy	If this bit is set, Status Modifier will also be set, indicating that the Control Unit was busy. The Control Unit was busy because: 1. A new command was initiated while the control unit was still erasing a track following a Format Write command. 2. On a dual access control unit configuration, the control unit was busy via the other I-O channel. 3. Busy, set without Status Modifier, will indicate Device Busy.
2.6	4	Channel End	Channel End indicates that the Channel-to-Control Unit operation is complete.
2.7	5	Device End	Device End will be presented with Channel End except in the case of a Seek command. Device End, in the case of a Seek, indicates the completion of Motion Control.

STATUS BYTE

	Bit Position	Description	Interpretation
2.8	6	Unit Check	An exceptional condition (but not necessarily an error) was detected. Additional information on this condition is contained in the Sense Bytes.
2.9	7	Unit Exception	This status results from a Data Length of zero in the Count Area of a record; and indicates End-of-File. When this condition is detected, information will be transferred from (or to) a (non-zero length) Key Area but not from (or to) the Data Area. This bit can be set on the following read commands: 1. TD Record 2. Count, Key and Data 3. Key and Data 4. Data This bit can be set on the following write commands: 1. Key and Data 2. Data

3. SENSE BYTES

3.1 Sense Byte 0

	Bit Position	Designation	Interpretation
3.1.1	Bit 0		1. Invalid Command. 2. Filemask is violated on a write command. 3. Two sets of file mask commands have been received in the same command chain. 4. A command code for a feature that is not installed. 5. A seek command with invalid address. 6. A command which makes an invalid sequence. 7. A seek command with less than 6 bytes of address. 8. Filemask in preceding read IPL in same chain.
3.1.2	Bit 1	Intervention Required	Device addressed is either physically or electrically nonexistant. After this status bit is set the program may try the same command again but not another command without causing other error.
3.1.3	Bit 2	Busout Check	Even parity appears on the output bus for data or command.
3.1.4	Bit 3	Equipment Check	Set by Sense Byte 2.
3.1.5	Bit 4	Data Check	Data error has been detected in the information received by the control unit from the device.
3.1.6	Bit 5	Overrun	The channel did not accept input information rapidly enough to assure the validity of the information. A byte was received too late, during writing, to be properly written. The remaining portion of the record area was filled with binary zero. Chained command was received too late to be properly executed. Overrun stops data transmission to or from the channel.
3.1.7	Bit 6	Track Condition Check	A read, write, or search command was attempted on a track which the flag byte indicates is defective. These commands are permitted, however, on home address and TD record.

SENSE BYTES (continued)

Sense Byte 0 (continued)

	Bit Position	Designation	Interpretation
3.1.7.1	Bit 6 (cont)	DEFECTIVE TRACK	1. Any read or search (except search HA, Read HA, Read RO) is attempted on the track in either multitrack or single track mode. The interrupt occurs prior to transmission of any data to or from the channel. 2. An overflow record being read, written, or searched overflows to a track flagged as defective. The interrupt occurs after the last byte on the previous track has been operated on and before the first byte for the defective track is requested from or to the channel.
3.1.7.2		ALTERNATE TRACK	1. A track condition check is generated when command chaining and multiple track mode signals indicate that operations are to continue on the next higher-order track or the record is not the last segment of an overflow record. 2. Track condition check inhibits the increment head switching.
3.1.8	Bit 7	SEEK CHECK	1. Transferred seek address is outside the valid address boundaries of the device. The unused bytes must contain zero. This condition also sets command reject. 2. Less than six bytes of seek address is sent. This also sets command reject. 3. Failure of hardware which results in the access mechanism failing to detent correctly. Mechanism going to either inner or outer stop. This case no command rejects. 4. On multi-track operation, the home address of the track advanced to does not compare with the physical address.

SENSE BYTES (continued)

3.2 Sense Byte 1

	Bit Position	Designation	Interpretation
3.2.1	Bit 0	Count Area Check	Data error in count area. Set data check.
3.2.2	Bit 1	Track Overrun	1. Writing has not been completed by the time the index point is detected. 2. Detected on Write RO, Write C-K-D, Write K-D, Write D, or Space Count.
3.2.3	Bit 2	End of Cylinder	CCW command chain has not been completed, but end of cylinder has been detected.
3.2.4	Bit 3	Invalid Sequence	Invalid Sequence of CCW.
3.2.5	Bit 4	No-Record-Found	1. An index passed condition is turned on whenever an index point is sensed on the device. 2. The index passed condition is turned off whenever the control unit performs a read operation in a HA or Data field area, any write command, a sense command, or any control command. 3. No-record-found condition occurs whenever the control unit senses an index point while performing a single track read or search operation other than Read RO or Read HA and the index passed latch is already on. 4. A no record found condition occurs when an index is sensed while executing a space count command following HA and no address mark is found. 5. A no-record-found condition occurs with missing address mark when neither HA or RO can be found on the track. 6. No-record-found is never set if the multi-track bit in the command is on.
3.2.6	Bit 5	File Protected	Seek, Write, Multi-track Read or Search command was issued that violated the file mask.
3.2.7	Bit 6	Missing Address Marker	This bit will be accompanied by bit 4 of Sense Byte 0 (Data Check). 1. 2 successive records in which bit 0 of the flag bytes were equal were read from the track; and there was no Index Marker between the 2 records. This is an indication that an Address Marker was missed. The Search ID command will inhibit detection of this condition, making it possible to pass over the missing Address Marker so that the remaining data on the track can be retrieved. 2. 2 index markers were passed without encountering any Address Markers.
3.2.8	Bit 7	Overflow	1. Overflow to a defective track. 2. Overflow from an alternate track. 3. Overflow to file protected bound. 4. Overflow to wrong track. 5. Data check in overflow record other than last record.

SENSE BYTES (continued)

3.3 Sense Byte 2

	Bit Position	Designation	Interpretation
3.3.1	Bit 0	Unsafe	This bit is used to indicate that a device malfunction has been detected. Some of these malfunctions are: More than one head has been selected. The device is trying to read and write at the same time. The write gate is Off and write driver is On. The write gate is On and write driver is Off. The erase driver is Off and the erase gate is On. The erase driver is On and the erase gate is Off. One of the DC file voltages has been lost.
3.3.2	Bits 1,2,3 and 4		Not used: always zero
3.3.3	Bit 5	Unselected Status	This bit indicates that some bit in the file status lines is on without being selected. This indicates a device malfunction of some kind since no bit should be on prior to selection.
3.3.4	Bits 6 and 7		Not used: always zero.

3.4 Sense Byte 3

Sense byte 3 indicates the present status of selected device.

Bit 0	Ready	The device is ready for operation.
Bit 1	On-line	The device is on-line.
Bit 2	Unsafe	The device malfunction has been detected.
Bit 3		Not used: always zero.
Bit 4		Not used: always one.
Bit 5	End of Cylinder	The end-of-cylinder has been detected.
Bit 6		Not used: always zero.
Bit 7	Seek Incomplete	The seek-incomplete condition has been detected.

SENSE BYTES (continued)

3.5 Sense Byte 4

This byte is always zero.

3.6 Sense Byte 5

This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). The codes in byte 5 indicate the type of command being executed when the overflow incomplete occurs. The codes and their meaning when the Unit Check (overflow incomplete sense) interruption occurs are:

Code in Hex.	Meaning
06	A read command was in progress.
05	A write command was in progress.
25	A search key-data-equal command was in progress, and the comparison is equal to this point.
45	A search key-data-high command was in progress, and the comparison is equal to this point.
65	A key-data-high command was in progress, and the comparison is equal to this point.
55	Any search key-data operation was in progress, and the comparison is low; or a search key-data equal was in progress, and the comparison was high.
75	A search key-data high or high-equal command was in progress, and the comparison is high.

See Record Overflow and Continue Scan for the programming usage of Sense byte 5 as command code.

3.7 Sense Bytes 6-31

Sense Bytes 6-31 are for on-line diagnostics and failure finding. A brief description of the sense bytes follows.

Sense Byte Number	Sense Byte Contains the Contents of:
6	Command Register
7	Head Register
8	Track Orientation Register
9	Unit Register
10	Gated Attention Encode
11	Data Length High Register
12	Data Length Low Register
13	Key Length Register
14	Flag Register
15	Mask Register
16	Cyclic Parity High Register

SENSE BYTES (continued)

Sense Bytes 6-31 (continued)

Sense Byte Number	Sense Byte Contains the Contents of:
17	Cyclic Parity Low Register
18	File Tag & Binary Counter High
19	Binary Counter Low
20	Cylinder Address Register
21	Status Register
22	File Bus Register
23	Adder Sum
24	Sequence Counter & Program Counter
25	Miscellaneous FF's
26	Queueing Register Stage 1
27	Queueing Register Stage 2
28	Queueing Register Stage 3
29	Data Register
30	X or Y Seek Register
31	Reserved

UNIVAC 9000 SERIES 600 CPM READER AND CONTROL

1. COMMAND REPERTOIRE

The following Command Codes may be issued to the Reader Control by the processor. Any other codes will be rejected and will return a Unit Check Status to the Processor.

P = Odd Parity Bit X = Ignored by Control Unit F = Detail Bit

	Bit Position P01234567	Command	Interpretation
1.1	PXX000000 or PXX110000	Test I-O	The Reader Control presents a status byte to the Channel. SERVICE OUT from the Channel clears the status.
1.2	PXX010000	Set Inhibit Status	This command is processed as a Test I-O Command. Status will be presented to the Channel and Inhibit Status In will be set.
1.3	PXX100000	Reset Inhibit Status	This command is processed as a Test I-O command. Status will be presented to the Channel and Inhibit Status In will be reset.
1.4	PXXXX0100	Sense	The Reader Control transfers from one to three sense bytes to the computer as input data. The first sense byte generally has details about any unusual conditions that occurred during the last operation. The channel can issue an early termination if the transfer of all sensebytes is not desired.
1.4.1			Prior to transmitting the sense data to the Channel, the Control Unit will test the Reader. The results of the test will modify the sense by setting additional flip-flops. The status will not be modified and no sense bits will be reset. Channel End and Device End will signal completion of the Sense Commands.
1.5	PAXXXXF10	Read	A = 0: Read data from the card and send to the Channel. Advance cards one station. At the completion of the data transfer, the Reader Control presents Status to the Channel. F = 0: Read in translate mode. F = 1: Read in image mode.

COMMAND REPERTOIRE (continued)

1.5.1 A = 1, F = 1 Maintenance mode read. Cards are advanced one station but card data is not read. Two bytes containing the following sixteen (16) special diagnostic status bits are sent as input data to the channel for maintenance purposes.

1.5.2

Data Byte 1	Bit	Diagnostic Designation
	0	Sector A
	1	Sector B
	2	Photocell 13
	3	Pinch Roller
	4	On-Off FF
	5	Feed FF
	6	Go FF
	7	Always 1

1.5.3

Data Byte 2	Bit	Diagnostic Designation
	0	25 ms Delay Flop
	1	11 ms Delay Flop
	2	Counter Bit 7
	3	Counter Bit 2
	4	Brake Peak
	5	Clutch Peak
	6	Clutch Hold
	7	Clutch/Brake Control

1.6 PXXXXXX11 Control No. OP. This code is used for diagnostics.

2. STATUS BYTE

2.1 The Status Byte supplies information pertaining to conditions of the last operation. The Status Byte will be presented to the Channel at the following times:

1. The end of the Initial Selection Sequence.
2. The completion of data transfers on the Read Command.

2.2 The status register will be cleared when the Channel responds to STATUS IN with SERVICE OUT. The following list defines use of the bits in the Status Byte.

	Bit Position	Designation	Interpretation
	P	Odd Parity	Parity for Status Byte.
2.3	0	Attention	Set by RUN switch.
2.4	1	Status Modifier	Normally set with the Busy bit to indicate that the Control Unit is busy performing a previously initiated command. Status Modifier will not be set with Busy if a new command is issued to the Control Unit when it is about to initiate an interrupt sequence to present end status from the previous operation.
2.5	2	Control Unit End	Not used. Bit always 0.
2.6	3	Busy	Indicates that the Control Unit cannot accept a Command because of one of the following reasons: a) Control is executing a previously iniated operation. b) Control is holding pending status conditions. NOTE: Condition (a) also presents the Status Modifier bit. Busy can occur only during the Initial Selection Sequence. Busy, due to pending status, will not be set if the command issued in (b) is a Test I-O.
2.7	4	Channel End	Channel End indicates the completion of the data transfers between the Control Unit and the Channel or the acceptance of a control command. If Channel End is "stacked," the Control Unit will disconnect and try to present the status when the priority allows. Channel End and Device End are presented together.
2.7.1			Following is a list of conditions which will present Channel End. a) The Control Unit will generate Channel End after the 80th column has been read. b) Acceptance of a Control Command.

STATUS BYTE (continued)

	Bit Position	Designation	Interpretation
2.8	5	Device End	Indicates the completion of a command initiated by the Channel and readiness to accept a new command. Device End and Channel End are presented together. In the Card Reader, Device End is presented in the following cases: Same as a) and b) for Channel End above.
2.9	6	Unit Check	One or more bits were set in Sense Byte 1 (bits 0 thru 7) when sampled with the setting of Channel End or Device End. A parity error in the Command Byte, an Invalid Command, or a Unit Abnormal, when tested in the Initial Selection Sequence, has been detected. In these cases, the Unit Check is sent to the Channel during the Initial Selection Sequence. The Reader was found to be non-ready when tested during Initial Selection. The command will be rejected and no end status will be generated. The normal sense bits will be set to indicate the type of error that occurred.
2.10	7	Unit Exception	Not used. Bit always 0.

3. SENSE BYTES

3.1 Sense data provides information about unusual conditions that occurred during the last operation. The sense information will be cleared when the next command is accepted if the command is not a Sense Command or a Test I-O.

3.2 Sense Byte 1

The status of various flip-flops in the Control Unit are transferred to this byte. This byte is used for error recovery routines or for maintenance functions in conjunction with failure finding routines.

Sense Byte 1

	Bit Position	Designation	Interpretation
3.2.1	P	Odd Parity	Parity bit for Sense Byte 1
3.2.2	0	Command Reject	An unspecified command was issued. This bit is suppressed if bad parity is detected during transfer of the command code. Neither Channel End nor Device End is set in the status.
3.2.3	1	Intervention Required	A Reader error, other than Read Check, was detected during the previous operation. The fault may be empty hopper, stacker full, misfeed, read jam, non-ready, or stacker jam.
3.2.4	2	BUS OUT Check	Parity error on the command transfer to the Control Unit. If the Control Unit is not holding pending status, a parity error during the command byte transfer causes immediate termination. Neither Device End nor Channel End will be set in the Status Byte. If the Control Unit is holding pending status, a parity error during the command byte transfer will be ignored. The sequence will be handled as if the Control Unit was holding pending status and the command byte had good parity.
3.2.5	3	Card Jam	A card transport error has occurred. A jam into the pre-read station, into the read station, or into the stacker will light the Feed Check indicator on the Reader Control Panel.
3.2.6	4	Data Check	A mispunched card, improper registration, or read head failure has been detected.
3.2.7	5	Overrun	New data has been read by Reader before SERVICE OUT has been received from the Channel for the data presently stored in the data register.
3.2.8	6	Inhibit Status In	Inhibit Status In is set.
3.2.9	7	Non-Repeat Abnormal	Hopper Empty, Stacker Full, Interlock Error, or Stacker Jam.

SENSE BYTE (continued)

3.3 Sense Bytes 2 and 3

The status of various flip-flops in the Control Unit are transferred to these bytes. Sense bytes 2 and 3 are used for maintenance analysis functions in conjunction with failure finding routines.

3.4 Sense Byte 2

Bit Position	Designation
0	Stop
1	Sector A
2	Status Acknowledge
3	Active
4	Read
5	Go
6	All on
7	On-Off FF

3.5 Sense Byte 3

Bit Position	Designation
0	Feed FF
1	Upper Cells Off
2	Lower Cells Off
3	Clutch/Brake Control
4	Initial Write
5	Sprocket C
6	Input to Motor Driver
7	Data Request

UNIVAC
DIVISION OF SPERRY RAND CORPORATION

SPECIFICATION REVISION RECORD

SHEET 19 | REVISION –

SPECIFICATION SYMBOL
SH04479

SPEC REV	EIR NO.	SHEET NO.	SHEET REV.	DESCRIPTION OF REVISION (DESCRIBE REVISION IN ONE OF THE FOLLOWING 3 WAYS) 1. ADDED ____ 2. DELETED ____ 3. CHANGED FROM ____ TO ____	CHG BY	CHCK	APPROVAL	DATE
–	H183386 -57	1-12 THRU 19	–	RELEASED IDENT. NO. -00.	G.J. 11-21-68			

```
0001                                *ESCR     PART 3841246-00  REV -   EIR M18386-57  LINES 0771   8/7/68
0002                                ESCR      START X'01F9'                                                  ESCR0000
0003    01F9                                  ORG   X'01F9'                                                  ESCR0010
0004                                *                                                                        ESCR0020
0005                                *                                                                        ESCR0030
0006                                ************************************************************************ ESCR0040
0007                                ************************************************************************ ESCR0050
0008                                *                                                                      * ESCR0060
0009                                *                                                                      * ESCR0070
0010                                *       ROUTINE ESCR     3 XIOFS - ENGINEER'S SPECIAL CONTROL ROUTINE * ESCR0080
0011                                *                                                                      * ESCR0090
0012                                *                                                                      * ESCR0100
0013                                ************************************************************************ ESCR0110
0014                                ************************************************************************ ESCR0120
0015                                *                                                                        ESCR0130
0016                                *                                                                        ESCR0140
0017                                *                                                                        ESCR0150
0018                                *                                                                        ESCR0160
0019                                *                                                                        ESCR0170
0020                                *                                                                        ESCR0180
0021                                *                                                                        ESCR0190
0022                                *                                                                        ESCR0200
0023                                *                                                                        ESCR0210
0024                                *                                                                        ESCR0220
0025                                *                                                                        ESCR0230
0026                                *                                                                        ESCR0240
0027                                *                                                                        ESCR0250
0028                                *                                                                        ESCR0260
0029                                *                                                                        ESCR0270
0030                                *                                                                        ESCR0280
0031                                *                                                                        ESCR0290
0032                                *                                                                        ESCR0300
0033                                *                                                                        ESCR0310
0034                                **   ALTER PARAMETER LOCATIONS BEGINNING IN LOCATION 1F9 AT INITIAL       ESCR0320
0035                                **   LOAD DISPLAY HALT OF 00EE.  CLEAR LOCATIONS 1D, 1E, 1F TO FF        ESCR0330
```

```
0036    **  BCW1 ADR   SET LOCATION 01FC TO 1 BYTE ADR OF BCW1 FOR C1-MX          ESCR0340
0037    **  BCW2 ADR   SET LOCATION 01FD TO 1 BYTE ADR OF BCW2 FOR C2-MX          ESCR0350
0038    **  BCW3 ADR   SET LOCATION 01FE TO 1 BYTE ADR OF BCW3 FOR C3-MX          ESCR0360
0039    **       DA    SET LOCATION 1FF TO DEVICE ADDRESS, COMMAND 1             ESCR0370
0040    **       DA    SET LOCATION 200 TO DEVICE ADDRESS, COMMAND 2             ESCR0380
0041    **       DA    SET LOCATION 201 TO DEVICE ADDRESS, COMMAND 3             ESCR0390
0042    **   COMMANDS  SET LOCATION 202 TO COMMAND 1                             ESCR0400
0043    **             SET LOCATION 203 TO COMMAND 2                             ESCR0410
0044    **             SET LOCATION 204 TO COMMAND 3                             ESCR0420
0045    **             SET LOCATION 205 TO OPTION SELECTION                      ESCR0430
0046    **         BIT  0 - 0 PHASE          9 TRACK, 1600 BPI                   ESCR0440
0047    **         BIT  0 - 1 NPZI           9 TRACK, 800 BPI                    ESCR0450
0048    **         BIT  1 - 0                DO NOT STOP BEFORE XIOF             ESCR0460
0049    **         BIT  1 - 1                STOP BEFORE XIOF TO ENABLE CYCLING  ESCR0470
0050    **         BIT  2 - 0                EXECUTE XIOF IN PM. 40 - 43 = STATUS ESCR0480
0051    **         BIT  2 - 1                EXECUTE XIOF IN IO. TIO FOR STATUS  ESCR0490
0052    **         BIT  3 - 0                DO NOT SET SIMULATE MODE            ESCR0500
0053    **         BIT  3 - 1                SET SIMULATE MODE                   ESCR0510
0054    **         BIT  4 - 0                EXECUTE COMMANDS 1,2,3 NORMALLY     ESCR0520
0055    **         BIT  4 - 1                EXECUTE COMMAND 1 - EXECUTE COMMANDS ESCR0530
0056    **                                   2 AND 3 ON ERROR. RESUME COMMAND 1  ESCR0540
0057    **         BIT  5 - 0                DO NOT PRINT ON ERROR               ESCR0550
0058    **         BIT  5 - 1                PRINT ON ERROR                      ESCR0560
0059    **         BIT  6 - 0                DO NOT UTILIZE DATA GENERATOR       ESCR0570
0060    **         BIT  6 - 1                UTILIZE DATA GENERATOR              ESCR0580
0061    **         BIT  7 - 0                DO NOT PRINT ON SUCCESSFUL TERM.    ESCR0590
0062    **         BIT  7 - 1                PRINT ON SUCCESSFUL TERMINATION     ESCR0600
0063    **   BCWS      SET LOCATIONS 206-9 TO BUFFER CONTROL WORD 1 IF MX CHAN.  ESCR0610
0064    **             SET LOCATIONS 20A-D TO BUFFER CONTROL WORD 2 IF MX CHAN.  ESCR0620
0065    **             SET LOCATIONS 20E-211 TO BUFFER CONTROL WORD 3 IF MX CHA  ESCR0630
0066    **   CAWS      SET LOCATIONS 218-21F SEL. CHAN. COMMAND WORD 1           ESCR0640
0067    **             SET LOCATIONS 220-227 SEL. CHAN. COMMAND WORD 2           ESCR0650
0068    **             SET LOCATIONS 228-22F SEL. CHAN. COMMAND WORD 3           ESCR0660
0069    **   DATA      SET LOCATIONS 230-237 TO DESIRED DATA PATTERN AND SET     ESCR0670
0070    **             OPT - BIT 6 TO 1                                          ESCR0680
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0071    01F9 07          TM1     DC    X'07'              TEST MASK FOR 2 INTS - DEVICE 1       ESCR0690
0072    01FA 07          TM2     DC    X'07'              TEST MASK FOR 2 INTS - DEVICE 2       ESCR0700
0073    01FB 07          TM3     DC    X'07'              TEST MASK FOR 2 INTS - DEVICE 3       ESCR0710
0074    01FC 70          MBC1    DC    X'70'              BCW1 ADDRESS                          ESCR0720
0075    01FD 70          MBC2    DC    X'70'              BCW3 ADDRESS                          ESCR0730
0076    01FE 70          MBC3    DC    X'70'              BCW3 ADDRESS                          ESCR0740
0077    01FF E0          DA00    DC    X'E0'              DEVICE ADDRESS - COMMAND 1            ESCR0750
0078    0200 E0          DA01    DC    X'E0'              DEVICE ADDRESS - COMMAND 2            ESCR0760
0079    0201 E0          DA02    DC    X'E0'              DEVICE ADDRESS - COMMAND 3            ESCR0770
0080    0202 012702      C123    DC    X'012702'          COMMAND SELECTION (3)                 ESCR0780
0081    0205 00          OPT     DC    X'00'              OPTION SELECTION                      ESCR0790
0082    0206 8040        BCW1    DC    X'8040'            64(10) = BYTE COUNT                   ESCR0800
0083    0208 1000                DC    Y(DAT1)            DATA ADDRESS = 1000(16)               ESCR0810
0084    020A 8040        BCW2    DC    X'8040'            64(10) = BYTE COUNT                   ESCR0820
0085    020C 2000                DC    Y(DAT2)            DATA ADDRESS = 2000(16)               ESCR0830
0086    020E 8040        BCW3    DC    X'8040'            64(10) = BYTE COUNT                   ESCR0840
0087    0210 3000                DC    Y(DAT3)            DATA ADDRESS = 3000(16)               ESCR0850
0088    0212 021A        CCW1    DC    Y(CW1+2)                                                 ESCR0860
0089    0214 0222        CCW2    DC    Y(CW2+2)                                                 ESCR0870
0090    0216 022A        CCW3    DC    Y(CW3+2)                                                 ESCR0880
0091    0218 0100100010000040    CW1     DC    X'0100100010000040'  WRITE 64 BYTES BEG. 1000, L FLAG  ESCR0890
0092    0220 0100200010000040    CW2     DC    X'0100200010000040'  WRITE 64 BYTES BEG. 2000, L FLAG  ESCR0900
0093    0228 0100300010000040    CW3     DC    X'0100300010000040'  WRITE 64 BYTES BEG. 3000, L FLAG  ESCR0910
0094    1000             DAT1    EQU   X'1000'                                                  ESCR0920
0095    2000             DAT2    EQU   X'2000'                                                  ESCR0930
0096    3000             DAT3    EQU   X'3000'                                                  ESCR0940
0097    0230 FFA9FF81D7A9FFA9    DATA    DC    X'FFA9FF81D7A9FFA9'                              ESCR0950
0098    0238 4412443A6C124412            DC    X'4412443A6C124412'                              ESCR0960
0099    0240 0100        RDT     DC    X'0100'          NUMBER OF TIMES 3 COMMANDS ARE REPEATED  ESCR0970
0100                     *                                                                      ESCR0980
0101                     *                                                                      ESCR0990
0102    0242 0000        IR8     DC    X'0000'                                                  ESCR1000
0103    0244 0005        BCW4    DC    X'0005'            NORMAL SENSE BUFFER CONTROL WORD MX   ESCR1010
0104    0246 0268                DC    Y(NSNS)                                                  ESCR1020
0105    0248 0005        BCW5    DC    X'0005'            MONITOR SENSE BUFFER CONTROL WORD MX  ESCR1030
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0106    024A 026D                          DC    Y(MSNS)                                                ESCR1040
0107    024C 0250                  CCW4    DC    Y(*+4)                                                 ESCR1050
0108    024E 0B00                  CW4     DC    X'0B00'          NORMAL SENSE COMMAND WORD - SEL       ESCR1060
0109    0250 0268                          DC    Y(NSNS)                                                ESCR1070
0110    0252 10000005                      DC    X'10000005'                                            ESCR1080
0111    0256 025A                  CCW5    DC    Y(*+4)                                                 ESCR1090
0112    0258 8B00                  CW5     DC    X'8B00'          MONITOR SENSE COMMAND WORD - SEL      ESCR1100
0113    025A 026D                          DC    Y(MSNS)                                                ESCR1110
0114    025C 10000005                      DC    X'10000005'                                            ESCR1120
0115    0260 FFFFFFFFFFFFFFFF      FF      DC    X'FFFFFFFFFFFFFFFF'                                    ESCR1130
0116    0268                       NSNS    DS    1CL5                                                   ESCR1140
0117    026D                       MSNS    DS    1CL5                                                   ESCR1150
0118    0272 0001                  D1      DC    X'0001'                                                ESCR1160
0119    0274 0100                  D256    DC    X'0100'                                                ESCR1170
0120    0276 3010                  DLIM    DC    X'3010'                                                ESCR1180
0121                               **                        PRESET INSTRUCTIONS                        ESCR1190
0122    0278 D201058A08E0          SCP0    MVC   HPR5-2(2),YCP    SUCCESSFUL COMMAND COMPLETION, PRNT   ESCR1200
0123    027E D201058C08E0                  MVC   INT2+8(2),YCP                                          ESCR1210
0124    0284 91200205                      TM    OPT,X'20'                                              ESCR1220
0125    0288 47100290                      BC    1,*+8                                                  ESCR1230
0126    028C 47F00380                      BC    15,TB2-4                                               ESCR1240
0127    0290 D20108B408E2                  MVC   RIOM+2(2),YCP+2                                        ESCR1250
0128    0296 47F00380                      BC    15,TB2-4                                               ESCR1260
0129    029A 470005E0              SPSP    BC    0,SPM                                                  ESCR1270
0130    029E 92F00298                      MVI   SPSP+1,X'F0'                                           ESCR1280
0131    02A2 920C08C8                      MVI   IS+2,X'0C'       RESET CHANNEL END, DEVICE END STATUS  ESCR1290
0132    02A6 47F00950                      BC    15,P*PR                                                ESCR1300
0133    02AA 47000000              SPSI    BC    0,0(,8)                                                ESCR1310
0134    02AE 92F002AB                      MVI   SPSI+1,X'F0'                                           ESCR1320
0135    02B2 920C08C8                      MVI   IS+2,X'0C'       RESET CHANNEL END, DEVICE END STATUS  ESCR1330
0136    02B6 47F00950                      BC    15,P*PR                                                ESCR1340
0137    02BA D20710000230          DGEN    MVC   DAT1(8),DATA                                           ESCR1350
0138    02C0 91080205                      TM    OPT,X'08'        IF OPT - BIT 4 IS SET, GENERATE       ESCR1360
0139    02C4 471002EA                      BC    1,D48K           8 K OF DATA FOR WRITE                 ESCR1370
0140    02C8 D2FF1008100B                  MVC   DAT1+8(256),DAT1                                       ESCR1380
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0141  02CE D2072000023@                MVC   DAT2(8),DATA                                  ESCR1390
0142  02D4 D2FF20002000                MVC   DAT2+8(256),DAT2                             ESCR1400
0143  02DA D2073000023@                MVC   DAT3(8),DATA                                 ESCR1410
0144  02E0 D2FF30003000                MVC   DAT3+8(256),DAT3                             ESCR1420
0145  02E6 47F00388                    BC    15,TB2+4                                     ESCR1430
0146  02EA 48F00208          D48K      LH    15,BCW1+2                                    ESCR1440
0147  02EE D207F0000238                MVC   8(8,15),DATA+8                               ESCR1450
0148  02F4 AAF00894                    AH    15,D16                                       ESCR1460
0149  02F8 D2FFF0001000      CGD       MVC   0(256,15),DAT1                               ESCR1470
0150  02FE AAF00274                    AH    15,D256                                      ESCR1480
0151  0302 49F00276                    CH    15,DLIM                                      ESCR1490
0152  0306 47800388                    BC    8,TB2+4                                      ESCR1500
0153  030A 47F002F8                    BC    15,CGD          CONTINUE GENERATING DATA     ESCR1510
0154  030E 92480541          SIMU      MVI   XIO+3,X'48'     SET SIMULATE MODE COMMAND    ESCR1520
0155  0312 D201007802AC                MVC   X'78'(2),CCW4                                ESCR1530
0156  0318 45800052E                   BAL   8,XIO-16        EXECUTE SIMULATE MODE COMMAND ESCR1540
0157  031C 47F00041A                   BC    15,SPC                                       ESCR1550
0158  0320 D2048CB10E20      SNRZ      MVC   S0+35(5),NESI   CORRECT SENSE TABLE FOR NRZI ESCR1560
0159  0326 D2090D060E25                MVC   S0+120(10),NESI+5                            ESCR1570
0160  032C D2090D150E2F                MVC   S0+135(10),NESI+15                           ESCR1580
0161  0332 D2590DC40E39                MVC   M0+110(90),NESI+25                           ESCR1590
0162  0338 92CB0541          NRZI      MVI   XIO+3,X'CB'     9 TRACK, NRZI, 800 BPI MODE SET ESCR1600
0163  033C D201007802AC                MVC   X'78'(2),CCW4                                ESCR1610
0164  0342 45800052E                   BAL   8,XIO-16        EXECUTE MODE COMMAND         ESCR1620
0165  0346 47F003F0                    BC    15,MS                                        ESCR1630
0166  034A A8600008          CKPC      LPSC  PSC6,X'60'      SET IO TO INDICATE UNSOLICITED INT. ESCR1640
0167  034E D201051A08C0                MVC   XIOF+4(2),LIM1+2 RESETS TO COMMAND 1         ESCR1650
0168  0354 920003ED                    MVI   CLSW+1,0        RESET STRT LOOP              ESCR1660
0169  0358 920004BB                    MVI   SPC-15,0        RESET SIMULATE AND NRZI SWITCHES ESCR1670
0170  035C D201031E0C8C                MVC   SNRZ-2(2),ARSM+2                             ESCR1680
0171  0362 920C08C8                    MVI   IS+2,X'0C'      RESET CE,DE FOR GENERAL CLEAR, STRT ESCR1690
0172  0366 D2000C501FC                 MVC   MX1+9(1),MBC1   SET ADDRESS OF BCW, COMMAND 1 ESCR1700
0173  036C D2000D501FD                MVC   MX2+9(1),MBC2   SET ADDRESS OF BCW, COMMAND 2 ESCR1710
0174  0372 D2000E501FE                MVC   MX3+9(1),MBC3   SET ADDRESS OF BCW, COMMAND 3 ESCR1720
0175  0378 91010205                   TM    OPT,1           PRINT ON SUCCESSFUL COMPLETION ESCR1730
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0176    037C 4710027C                BC    1,SCP0          OF COMMAND ?                        ESCR1740
0177    0380 91020205                TM    OPT,X'02'       DATA GENERATOR REQUESTED            ESCR1750
0178    0384 471002BA        TB2     BC    1,DGEN                                              ESCR1760
0179    0388 91200205                TM    OPT,X'20'        PM OR IO MODE FOR XIOF?            ESCR1770
0180    038C 4710067A                BC    1,EXIO                                              ESCR1780
0181    0390 91080205                TM    OPT,X'08'       IS SPECIAL ERROR RECOVERY DESIRED   ESCR1790
0182    0394 4710083C                BC    1,RCVY                                              ESCR1800
0183    0398 48A008E4                LH    10,LDA                                              ESCR1810
0184    039C D20902680267    STRT    MVC   NSNS(10),NSNS-1 CLEAR SENSE INFORMATION             ESCR1820
0185    03A2 D205007A0260            MVC   X'7A'(6),FF     CLEAR SEL CHANNEL CAW               ESCR1830
0186    03A8 D2030040026C            MVC   X'40'(4),FF     CLEAR INT. LOCATIONS                ESCR1840
0187    03AE 92FF08CA                MVI   DS,X'FF'        CLEAR DS                            ESCR1850
0188    03B2 D2000693A006            MVC   TIO1+1(1),6(10) SET DA IN TIO1                      ESCR1860
0189    03B8 D20006DFA006            MVC   TIO2+1(1),6(10) SET DA IN TIO2                      ESCR1870
0190    03BE D200053FA006            MVC   XIO+1(1),6(10)  SET DA IN XIOF                      ESCR1880
0191    03C4 D20008C9A006            MVC   IS+3(1),6(10)   SET DA IN STATUS COMPARE AREA       ESCR1890
0192    03CA D20007A5A003            MVC   MXS+3(1),3(10)  SET BCW ADDRESS IN SENSE CONTROLS   ESCR1900
0193    03D0 D20007F9A003            MVC   SELS-7(1),3(10)                                     ESCR1910
0194    03D6 D2000AFFA003            MVC   EMX+5(1),3(10)  SET BCW ADDRESS FOR EDITING ON PRINT ESCR1920
0195    03DC D200057BA000            MVC   HPR5-17(1),0(10) SET TM CONTROL FOR PM              ESCR1930
0196    03E2 D20006ABA000            MVC   SDS+1(1),0(10)  SET TM CONTROL FOR IO               ESCR1940
0197    03E8 AAA00272                AH    10,D1                                               ESCR1950
0198    03EC 4700F000        CLSW    BC    0,0(,15)                                            ESCR1960
0199    03F0 9180A005        MS      TM    5(10),X'80'     DA INDICATES SHARED MX CHANNEL?     ESCR1970
0200    03F4 471004BC                BC    1,MX1                                               ESCR1980
0201    03F8 9120A005                TM    5(10),X'20'     DA INDICATES MX OR SEL CHANNEL?     ESCR1990
0202    03FC 478004BC                BC    8,MX1                                               ESCR2000
0203    0400 D20008C6A005            MVC   IS(1),5(10)     SET IS TO CORRECT SEL CHAN VALUE    ESCR2010
0204    0406 920008C7                MVI   IS+1,0          SET IS + 1 TO CORRECT SEL CHAN VALUE ESCR2020
0205    040A 47000422                BC    0,SPC+8         SKIP SIMULATE AND NRZI              ESCR2030
0206    040E 92F0040B                MVI   *-3,X'F0'                                           ESCR2040
0207    0412 91100205                TM    OPT,X'10'       IS SIMULATION INDICATED             ESCR2050
0208    0416 4710038E                BC    1,SIMU                                              ESCR2060
0209    041A 91800205        SPC     TM    OPT,X'80'       PHASE OR NRZI                       ESCR2070
0210    041E 4710032C                BC    1,SNRZ                                              ESCR2080
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0211    0422 D20100780212           MVC   X'78'(2),CCW1     SET CAW TO COMMAND WORD 1          ESCR2090
0212    0428 45800516               BAL   8,XIOF            EXECUTE COMMAND 1                  ESCR2100
0213    042C A90000C1       HPR1    HPR   X'00C1'           COMMAND 1 EXECUTED - SEL. CHANNEL  ESCR2110
0214    0430 9247042C               MVI   HPR1,X'47'        RESET HALT AT COMMAND 1            ESCR2120
0215    0434 47800398               BC    8,STRT-4                                             ESCR2130
0216    0438 9180A006               TM    6(10),X'80'       DA INDICATES SHARED MX CHANNEL?    ESCR2140
0217    043C 471004CC               BC    1,MX2                                                ESCR2150
0218    0440 9120A006               TM    6(10),X'20'       DA INDICATES MX OR SEL CHANNEL?    ESCR2160
0219    0444 478004CC               BC    8,MX2                                                ESCR2170
0220    0448 D20008C6A006           MVC   IS(1),6(10)       SET IS TO CORRECT SEL CHAN VALUE   ESCR2180
0221    044E 920008C7               MVI   IS+1,0            SET IS + 1 TO CORRECT SEL CHAN VALUE ESCR2190
0222    0452 D20100780214           MVC   X'78'(2),CCW2     SET CAW TO COMMAND WORD 2          ESCR2200
0223    0458 92F003ED       SEL2    MVI   CLSW+1,X'F0'      SET CLSW SWITCH                    ESCR2210
0224    045C 92000521               MVI   XIOF+11,0                                            ESCR2220
0225    0460 45F0039C               BAL   15,STRT           PRESET CONDITIONS                  ESCR2230
0226    0464 920008B5               MVI   RIOM+3,0          SWITCH FOR RESETTING OPT BIT 4 TO C1 ESCR2240
0227    0468 91080285               TM    OPT,X'08'                                            ESCR2250
0228    046C 471004EC               BC    1,SRC2                                               ESCR2260
0229    0470 45800516               BAL   8,XIOF            EXECUTE COMMAND 2                  ESCR2270
0230    0474 A90000C2       HPR2    HPR   X'00C2'           COMMAND 2 EXECUTED - SEL. CHANNEL  ESCR2280
0231    0478 92470474               MVI   HPR2,X'47'        RESET HALT AT COMMAND 2            ESCR2290
0232    047C 9180A006               TM    6(10),X'80'       DA INDICATES SHARED MX CHANNEL?    ESCR2300
0233    0480 471004DC               BC    1,MX3                                                ESCR2310
0234    0484 9120A006               TM    6(10),X'20'       DA INDICATES MX OR SEL CHANNEL?    ESCR2320
0235    0488 478004DC               BC    8,MX3                                                ESCR2330
0236    048C D20008C6A006           MVC   IS(1),6(10)       SET IS TO CORRECT SEL CHAN VALUE   ESCR2340
0237    0492 920008C7               MVI   IS+1,0            SET IS + 1 TO CORRECT SEL CHAN VALUE ESCR2350
0238    0496 D20100780216           MVC   X'78'(2),CCW3     SET CAW TO COMMAND WORD 3          ESCR2360
0239    049C 45F0039C       SEL3    BAL   15,STRT           PRESET CONDITIONS                  ESCR2370
0240    04A0 45800516               BAL   8,XIOF            EXECUTE COMMAND 3                  ESCR2380
0241    04A4 A90000C3       HPR3    HPR   X'00C3'           COMMAND 3 EXECUTED - SEL. CHANNEL  ESCR2390
0242    04A8 924704A4               MVI   HPR3,X'47'        RESET HALT AT COMMAND 3            ESCR2400
0243    04AC 45F00398               BAL   15,STRT-4         PRESET CONDITIONS                  ESCR2410
0244    04B0 91080285               TM    OPT,X'08'                                            ESCR2420
0245    04B4 471004F4               BC    1,SRC1                                               ESCR2430
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0246  04B8 47F003F0          BC    15,MS              REPEAT                                  ESCR2440
0247  04BC D20108C60260  MX1  MVC   IS(2),FF          SET IS,IS+1 TO CORRECT MX CHAN VALUE    ESCR2450
0248  04C2 D2030070028E       MVC   X'70'(4),BCW1      SET BCW1                                ESCR2460
0249  04C8 47F0040A          BC    15,SPC-16                                                  ESCR2470
0250  04CC D20108C60260  MX2  MVC   IS(2),FF          SET IS,IS+1 TO CORRECT MX CHAN VALUE    ESCR2480
0251  04D2 D2030070029A       MVC   X'70'(4),BCW2      SET BCW2                                ESCR2490
0252  04D8 47F00458          BC    15,SEL2                                                    ESCR2500
0253  04DC D20108C60260  MX3  MVC   IS(2),FF          SET IS,IS+1 TO CORRECT MX CHAN VALUE    ESCR2510
0254  04E2 D2030070029E       MVC   X'70'(4),BCW3      SET BCW3                                ESCR2520
0255  04E8 47F0049C          BC    15,SEL3                                                    ESCR2530
0256  04EC A6010051A  SRC2   AI    XIOF+4,1                                                   ESCR2540
0257  04F0 47F00470          BC    15,HPR2-4                                                  ESCR2550
0258  04F4 92F00521  SRC1   MVI   XIOF+11,X'F0'                                              ESCR2560
0259  04F8 47F003F0          BC    15,MS              REPEAT                                  ESCR2570
0260  04FC D2010051A08C0 RC   MVC   XIOF+4(2),LIM1+2                                         ESCR2580
0261  0502 47F0052E          BC    15,XIO-16                                                  ESCR2590
0262                       *                                                                ESCR2600
0263                       ***   ISSUE START INPUT-OUTPUT COMMAND, CHECKING FOR ACCEPTANCE  *** ESCR2610
0264  0506 A8500512          LPSC  YIOU-2,X'50'                                             ESCR2620
0265  050A A8600D8  IOUI   LPSC  PSC6,X'60'          IO MODE UNSOLICITED INTERRUPTS          ESCR2630
0266  050E 47F0050E          BC    15,*                                                       ESCR2640
0267  0512 0000              DC    X'0000'                                                    ESCR2650
0268  0514 050E      YIOU   DC    Y(IOUI+4)                                                  ESCR2660
0269  0516 D2000541020C2 XIOF  MVC   XIO+3(1),C123     SET UP COMMAND                          ESCR2670
0270  051C A6010051A          AI    XIOF+4,1                                                   ESCR2680
0271  0520 47000FC           BC    0,RC                                                       ESCR2690
0272  0524 D501051A08BE       CLC   XIOF+4(2),LIM1                                           ESCR2700
0273  052A 47800FC           BC    8,RC               RESET TO FIRST COMMAND                  ESCR2710
0274  052E A8600BA           LPSC  PSC1,X'60'         SET IO INT. RETURN. STAY IN PM          ESCR2720
0275  0532 91400205          TM    OPT,X'40'           CHECK TO SEE IF HALT BEFORE XIOF       ESCR2730
0276  0536 4780053E          BC    8,XIO               IS DESIRED                             ESCR2740
0277  053A A900053A          HPR   *                  HALT BEFORE XIOF                        ESCR2750
0278  053E A4E00001  XIO    XIOF  1,X'E0'            XIOF COMMAND EXECUTION                  ESCR2760
0279  0542 4780054E          BC    8,*+12                                                     ESCR2770
0280  0546 A900054C  HPR4   HPR   *                  COMMAND NOT ACCEPTED                    ESCR2780
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0281    054A 47F0054A                  BC    15,*              RECOVERY SWITCH                              ESCR2790
0282    054E 47F0054E          LOOP    BC    15,*              WAIT FOR INTERRUPT - PM SET                  ESCR2800
0283                           **      BC    15,TI01           BRANCH TO TI0 - IO SET                       ESCR2810
0284    0552 47F0054E                  BC    15,LOOP                                                        ESCR2820
0285                           *                                                                           ESCR2830
0286                           ***     ANALYZE STATUS GENERATED BY PROCESSOR MODE INTERRUPTS          *** ESCR2840
0287    0556 D5010002073G      INT     CLC   X'02'(2),YXIO                                                 ESCR2850
0288    055C 4740072E                  BC    4,HPRA                                                       ESCR2860
0289    0560 D5010002073G              CLC   X'02'(2),YXIO+2                                              ESCR2870
0290    0566 47C005EE                  BC    12,UINT                                                      ESCR2880
0291    056A 91800042                  TM    X'42',X'80'                                                  ESCR2890
0292    056E 471005EE                  BC    1,UINT            HANDLE AS UNSOLICITED INTERRUPT            ESCR2900
0293    0572 9503053F                  CLI   XIO+1,3           INTERNAL DEVICE STATUS EXPECTED?           ESCR2910
0294    0576 47C005D8                  BC    12,ES00                                                      ESCR2920
0295    057A 91070541                  TM    XIO+3,X'07'       COMMAND EXPECTS 2 INTERRUPTS               ESCR2930
0296    057E 47100598                  BC    1,IN22                                                       ESCR2940
0297    0582 D503004008C6              CLC   X'40'(4),IS       COMPARE STATUS                             ESCR2950
0298    0588 478005E0                  BC    8,SPM             COMMAND IS COMPLETED SUCCESSFULLY          ESCR2960
0299    058C A900058C          HPR5    HPR   *                 COMMAND WAS IN ERROR. CK 40 THRU 43        ESCR2970
0300    0590 47F0084C                  BC    15,GRPM                                                      ESCR2980
0301    0594 47F00594                  BC    15,*              RECOVERY SWITCH                            ESCR2990
0302    0598 9200080C8         IN22    MVI   IS+2,X'08'        SET UP CE STATUS COMPARE                   ESCR3000
0303    059C D503004008C6              CLC   X'40'(4),IS       COMPARE CE STATUS                          ESCR3010
0304    05A2 478005B6                  BC    8,L4DE            CHANNEL END STATUS OK. LOOK FOR DE         ESCR3020
0305    05A6 920C08C8                  MVI   IS+2,X'0C'        RESET STATUS TO EXPECT CE,DE               ESCR3030
0306    05AA A90005AA          HPR6    HPR   *                 CE STATUS EXPECTED. CK 40 THRU 43          ESCR3040
0307    05AE 47F0084C                  BC    15,GRPM                                                      ESCR3050
0308    05B2 47F005B2                  BC    15,*              RECOVERY SWITCH                            ESCR3060
0309    05B6 920408C8          L4DE    MVI   IS+2,X'04'        SET UP DE STATUS COMPARE                   ESCR3070
0310    05BA A84800C2                  LPSC  PSC2,X'40'        SET PM TO LOOP WAITING FOR 2ND INT.        ESCR3080
0311    05BE D503004008C6      INT2    CLC   X'40'(4),IS       COMPARE DE STATUS                          ESCR3090
0312    05C4 478005E0                  BC    8,SPM             COMMAND IS COMPLETED SUCCESSFULLY          ESCR3100
0313    05C8 920C08C8                  MVI   IS+2,X'0C'        RESET STATUS TO EXPECT CE,DE               ESCR3110
0314    05CC A900058C          HPR7    HPR   *                 DE STATUS EXPECTED. CK 40 THRU 43          ESCR3120
0315    05D0 47F0084C                  BC    15,GRPM                                                      ESCR3130
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0316    05D4 47F005D4                  BC    15,*              RECOVERY SWITCH                          ESCR3140
0317    05D8 920008C8          ES00    MVI   IS+2,0            SET EXPECTED STATUS TO 00 AND LOOK       ESCR3150
0318    05DC 47F00582                  BC    15,HPR5-10        FOR ONLY ONE INTERRUPT                   ESCR3160
0319    05E0 920C08C8          SPM     MVI   IS+2,X'0C'        RESET CHANNEL END, DEVICE END STATUS     ESCR3170
0320    05E4 D2020301D0260             MVC   X'1D'(3),FF       CLEAR MX CHAN ERROR LOCATIONS            ESCR3180
0321    05EA A84008CC                  LPSC  PSC3,X'48'        SET PM                                   ESCR3190
0322    05EE D50100020788      UINT    CLC   2(2),YPR1+4       DETERMINE PRINTER SITUATION              ESCR3200
0323    05F4 47200616                  BC    2,NPHI                                                     ESCR3210
0324    05F8 D5010002078A              CLC   2(2),YPR1                                                  ESCR3220
0325    05FE 474006l6                  BC    4,NPHI                                                     ESCR3230
0326    0602 D5010002078C              CLC   2(2),YPR1+2                                                ESCR3240
0327    0608 47800758                  BC    8,PXHI                                                     ESCR3250
0328    060C D2010914078D      PRIU    MVC   PEXT+2(2),YPRI    PRINTER IS IN USE                        ESCR3260
0329    0612 A8700000                  LPSC  0,X'70'           RETURN TO PROCESS AT INT POINT, IO       ESCR3270
0330    0616 D2830ED80000      NPHI    MVC   SPA(132),X'80'    STORE PRINTER AREA                       ESCR3280
0331    061C 45C00942                  BAL   12,CPAR                                                    ESCR3290
0332    0620 D21700800EB1              MVC   X'80'(24),EUI     EDIT UNSOLICITED INTERRUPT               ESCR3300
0333    0626 45C00B6E                  BAL   12,EDS            EDIT DEVICE STATUS                       ESCR3310
0334    062A 45C008E6                  BAL   12,PRNT                                                    ESCR3320
0335    062E D2830080ED8               MVC   X'80'(132),SPA    RESTORE PRINTER AREA                     ESCR3330
0336    0634 91800538                  TM    XIO+1,X'80'       DA INDICATES SHARED MX CHANNEL?          ESCR3340
0337    0638 47100768                  BC    1,R401                                                     ESCR3350
0338    063C 91200538                  TM    XIO+1,X'20'       DA INDICATES MX OR SEL CHANNEL?          ESCR3360
0339    0640 47800768                  BC    8,R401                                                     ESCR3370
0340    0644 A9000644                  HPR   *           IO STILL SET.  UNEXPECTED INTERRUPT            ESCR3380
0341                           *                                OR PREVIOUS LPSC DID NOT WORK          ESCR3390
0342    0648 D5010002050C      DRET    CLC   X'02'(2),YIOU                                              ESCR3400
0343    064E 47800536                  BC    8,XIO                                                      ESCR3410
0344    0652 D5010002072E              CLC   X'02'(2),YXIO                                              ESCR3420
0345    0658 47400672                  BC    4,UIRT-4                                                   ESCR3430
0346    065C D5010002072A              CLC   X'02'(2),YXIO+4                                            ESCR3440
0347    0662 47200672                  BC    2,UIRT-4                                                   ESCR3450
0348    0666 A8600B8A                  LPSC  PSC1,X'60'        SET IO INT RETURN TO INT. SET PM.        ESCR3460
0349    066A A900066A                  HPR   *                 PREVIOUS LPSC DID NOT SWITCH TO PM.      ESCR3470
0350                           *                                IF INTERRUPTED, CONTROL DID NOT GO       ESCR3480
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                                    *                                      LOCATION INT.                        ESCR3490
          066E 47F00644                      BC     15,DRET-4                                                   ESCR3500
          0672 47000672                      BC     0,*                   RECOVERY SWITCH                      ESCR3510
          0676 A86000D8             UIRT     LPSC   PSC6,X'60'            LOAD IO PSC TO EXPECT OTHER          ESCR3520
                                    *  UNSOLICITED INTERRUPTS. RETURN TO PM AT POINT OF LAST INTERRUPT       * ESCR3530
                                    *                                                                         ESCR3540
                                    ***      ANALYZE INHIBITED STATUS GENERATED BY XIOFS AND UNSOLICITED  *** ESCR3550
                                    ***                                    INTERRUPT CONDITIONS.           *** ESCR3560
          067A D201052E00DC         EXIO     MVC    XIO-16(2),IOC          SET UP FOR IO MODE                   ESCR3570
          0680 D201055000DE                  MVC    LOOP+2(2),IOC+2                                             ESCR3580
          0686 A87000D4                      LPSC   PSC5,X'70'             SET IO MODE                          ESCR3590
          068A A900068A                      HPR    *                      IO MODE NOT SET                      ESCR3600
          068E 47F0068E                      BC     15,*                   RECOVERY SWITCH                      ESCR3610
          0692 A5E000CA             TIO1     TIO    DS,X'E0'                                                    ESCR3620
          0696 47200692                      BC     2,TIO1                 LOOP ON TIO TILL BUSY STATUS DROPS   ESCR3630
          069A 4740070E                      BC     4,SDSC                 NON-ZERO STATUS IS STORED            ESCR3640
          069E A900069E                      HPR    *                      BUSY STATUS IS FOLLOWED BY ZERO DS   ESCR3650
          06A2 47F0086C                      BC     15,GRIO                                                     ESCR3660
          06A6 47F006A6                      BC     15,*                   RECOVERY SWITCH                      ESCR3670
          06AA 91070541             SDS      TM     XIO+3,X'07'            COMMAND EXPECTS 2 INTERRUPTS?        ESCR3680
          06AE 471006C6                      BC     1,HPR8+12                                                   ESCR3690
          06B2 950C00CA                      CLI    DS,X'0C'               COMPARE CE DE STATUS                 ESCR3700
          06B6 478008B2                      BC     8,RIOM                                                      ESCR3710
          06BA A90006BA             HPR8     HPR    *                      COMMAND STATUS NOT CE,DE. CK LOC DS  ESCR3720
          06BE 47F0086C                      BC     15,GRIO                                                     ESCR3730
          06C2 47F006C2                      BC     15,*                   RECOVERY SWITCH                      ESCR3740
          06C6 950800CA                      CLI    DS,X'08'               COMPARE CE STATUS                    ESCR3750
          06CA 478006DE                      BC     8,*+20                                                      ESCR3760
          06CE 920C00C8                      MVI    IS+2,X'0C'            RESET STATUS TO EXPECT CE,DE         ESCR3770
          06D2 A90006D2                      HPR    *                      BUSY STATUS IS FOLLOWED BY NO CE     ESCR3780
          06D6 47F0086C                      BC     15,GRIO                                                     ESCR3790
          06DA 47F006DA                      BC     15,*                   RECOVERY SWITCH                      ESCR3800
          06DE A5E000CB             TIO2     TIO    DS+1,X'E0'             THIS 2ND TIO SHOULD STORE DE STATUS  ESCR3810
          06E2 474006F6                      BC     4,*+20                                                      ESCR3820
          06E6 920C00C8                      MVI    IS+2,X'0C'            RESET STATUS TO EXPECT CE,DE         ESCR3830
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0386  06EA A90006EA            HPR   *                CC NOT 01 ON 2ND TIO FOR DE STATUS   ESCR3840
0387  06EE 47F0086C            BC    15,GRIO                                               ESCR3850
0388  06F2 47F006F2            BC    15,*             RECOVERY SWITCH                      ESCR3860
0389  06F6 950408CB            CLI   DS+1,X'04'       COMPARE DE STATUS                    ESCR3870
0390  06FA 478008B2            BC    8,RIOM                                                ESCR3880
0391  06FE 920C08C8            MVI   IS+2,X'0C'       RESET STATUS TO EXPECT CE,DE         ESCR3890
0392  0702 A9000702            HPR   *                DS+1 NOT DE STATUS                   ESCR3900
0393  0706 47F0086C            BC    15,GRIO                                               ESCR3910
0394  070A 47F0070A            BC    15,*             RECOVERY SWITCH                      ESCR3920
0395  070E 9503053F  SDSC      CLI   XIO+1,3          INTERNAL DEVICE STATUS EXPECTED?     ESCR3930
0396  0712 47C0071A            BC    12,CDS0                                               ESCR3940
0397  0716 47F006AA            BC    15,SDS                                                ESCR3950
0398  071A 95FB08CA  CDS0      CLI   DS,X'FB'         COMPARE STATUS(INTERNAL DEVICE) TO 0 ESCR3960
0399  071E 478008B2            BC    8,RIOM           OR BIT 5(INTERRUPT REQUEST PENDING)  ESCR3970
0400  0722 A9000722  HPR9      HPR   *                COMMAND STATUS NOT 00 OR 04 FOR      ESCR3980
0401                 *                               INTERNAL DEVICE                    * ESCR3990
0402  0726 47F0086C            BC    15,GRIO                                               ESCR4000
0403  072A 47F0072A            BC    15,*             RECOVERY SWITCH                      ESCR4010
0404  072E A900072E  HPRA      HPR   *                AN INT SHOULD NOT GIVE CONTROL TO    ESCR4020
0405  0732 47F0072E            BC    15,HPRA          LOC TAGGED INT FROM SUCH AN ADDRESS. ESCR4030
0406  0736 0532      YXIO      DC    Y(XIO-12)                                             ESCR4040
0407  0738 054A                DC    Y(XIO+12)        INT SHOULD NOT BE FROM THIS XIOF.    ESCR4050
0408                 *                               PRINT UINT AND RETURN TO THIS POINT. ESCR4060
0409  073A 0552                DC    Y(LOOP+4)                                             ESCR4070
0410  073C D2010914094E  IWP   MVC   PEXT+2(2),P*PR-2 RESTORE PRINTER EXIT               ESCR4080
0411  0742 D201078C0028        MVC   IR12(2),X'28'    HOLD PM IR12                         ESCR4090
0412  0748 D2030672077B        MVC   EXIO-8(4),ISW1                                        ESCR4100
0413  074E 47F0061C            BC    15,NPHI+6                                             ESCR4110
0414  0752 D2030672077C        MVC   EXIO-8(4),ISW1+4                                      ESCR4120
0415  0758 A840078A            LPSC  IR12-2,X'40'     SET PM, RETURN TO NORMAL PRINT EXIT  ESCR4130
0416  075C 95801000  PXHI      CLI   0(1),X'80'                                            ESCR4140
0417  0760 4780060C            BC    8,PRIU                                                ESCR4150
0418  0764 D2010914078B        MVC   PEXT+2(2),YPRI   PRINTER IS IN USE.  XIOF REJ. CASE  ESCR4160
0419  076A 47F008EA            BC    15,PRNT+4                                             ESCR4170
0420  076E D2010B400260  R401  MVC   X'40'(2),FF      CLEAR 40, 41 SET BY UNSOLICITED INT. ESCR4180
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0421  0774 47F0066E            BC    15,EXIO-12                                    ESCR4190
0422  0778 47F00752    ISW1    BC    15,IWP+22                                     ESCR4200
0423  077C 47000672            BC    0,EXIO-8                                      ESCR4210
0424  0780 073C        YPRI    DC    Y(IWP)          INTERRUPT WHILE PRINTING      ESCR4220
0425  0782 08FA                DC    Y(PRNT+20)                                    ESCR4230
0426  0784 08FE        YPR1    DC    Y(PRNT+24)                                    ESCR4240
0427  0786 0916                DC    Y(P*00-4)                                     ESCR4250
0428  0788 0942                DC    Y(CPAR)                                       ESCR4260
0429  078A 0000                DC    X'0000'                                       ESCR4270
0430  078C 0000        IR12    DC    X'0000'                                       ESCR4280
0431                   *                                                           ESCR4290
0432                   **    CODING TO OBTAIN SENSE AND MONITOR SENSE INFORMATION  ** ESCR4300
0433  078E A84000D0            LPSC  PSC4,X'40'      SET PM - ENTER IN IO DUE TO ERROR ESCR4310
0434  0792 47F005EE            BC    15,UINT         PM NOT SET OR UNSOLICITED INTERRUPT ESCR4320
0435  0796 47F00796            BC    15,*            RECOVER SWITCH                ESCR4330
0436  079A 40000242    GSW     STH   8,IR8           GET SENSE WORDS               ESCR4340
0437  079E 92040541            MVI   XIO+3,X'04'                                   ESCR4350
0438  07A2 D2030070024A MXS     MVC   X'70'(4),BCW4   SET NORMAL SENSE COMMAND UP - MX ESCR4360
0439  07A8 D2010078024C        MVC   X'78'(2),CCW4   SET NORMAL SENSE COMMAND - SEL ESCR4370
0440  07AE 4580052E            BAL   8,XIO-16                                      ESCR4380
0441  07B2 D200026D053F        MVC   MSNS(1),XIO+1   STORE CURRENT DA              ESCR4390
0442  07B8 94E0026D            NI    MSNS,X'E0'      ERASE DEVICE NUMBER           ESCR4400
0443  07BC 9560026D            CLI   MSNS,X'60'      MAGNETIC TAPES ON SELECTOR CHANNEL - ESCR4410
0444  07C0 478007D8            BC    8,GMS+4         DA EQUAL 60 - 6F              ESCR4420
0445  07C4 95E0026D            CLI   MSNS,X'E0'      MAGNETIC TAPES ON CHANNEL     ESCR4430
0446  07C8 478007D8            BC    8,GMS+4         DA EQUAL E0 - EF              ESCR4440
0447  07CC 95C0026D            CLI   MSNS,X'C0'      MAGNETIC TAPES ON MX CHANNEL - ESCR4450
0448  07D0 47800B96            BC    8,E46C                                        ESCR4460
0449  07D4 47F0082C    GMS     BC    15,PRSW-4                                     ESCR4470
0450  07D8 920800A2F           MVI   SSBE+1,8        SET SENSE BYTE-BIT-EDIT SWITCH ESCR4480
0451  07DC D2000541025B        MVC   XIO+3(1),CW5    SET MONITOR MODE COMMAND      ESCR4490
0452  07E2 D2010078024C        MVC   X'78'(2),CCW4                                 ESCR4500
0453  07E8 4580052E            BAL   8,XIO-16                                      ESCR4510
0454  07EC 92040541            MVI   XIO+3,X'04'     SET SENSE COMMAND             ESCR4520
0455  07F0 D2010078025B        MVC   X'78'(2),CCW5   SET MONITOR SENSE COMMAND UP - SEL ESCR4530
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0456    07F6 D203007700248                MVC   X'70'(4),BCW5      SET MONITOR SENSE COMMAND UP - MX    ESCR4540
0457    07FC 4560052E                     BAL   6,XIO-16                                             ESCR4550
0458    0800 47000000           SELS      BC    0,*                DISPLAY SENSE INFORMATION SWITCH  ESCR4560
0459    0804 D2000541024E                 MVC   XIO+3(1),CW4       SET RESET MONITOR MODE COMMAND    ESCR4570
0460    080A D201007B024C                 MVC   X'7B'(2),CCW4                                        ESCR4580
0461    0810 4560052E                     BAL   6,XIO-16                                             ESCR4590
0462    0814 91100205                     TM    OPT,X'10'           SIMULATE SET?                    ESCR4600
0463    0818 4780082C                     BC    8,PRSW-4                                             ESCR4610
0464    081C D201031E0C8A       RSIM      MVC   SIMU+16(2),ARSM                                      ESCR4620
0465    0822 47F0030E                     BC    15,SIMU                                              ESCR4630
0466    0826 D201031E04BA                 MVC   SIMU+16(2),MX1-2                                     ESCR4640
0467    082C 48600242                     LH    6,IR8               RESUME TEST                      ESCR4650
0468    0830 47000A08           PRSW      BC    0,EGS+24                                             ESCR4660
0469    0834 47F08000                     BC    15,0(,8)                                             ESCR4670
0470    0838 92F00435           RCVY      MVI   HPR1+9,X'F0'        SET OPT - BIT 4 SWITCH SEL       ESCR4680
0471    083C 92F00521                     MVI   XIOF+11,X'F0'                                        ESCR4690
0472    0840 92F009C1                     MVI   ECC-25,X'F0'        EDIT CW1 ONLY                    ESCR4700
0473    0844 92F00B11                     MVI   EMX+23,X'F0'        EDIT BCW1 ONLY                   ESCR4710
0474    0848 47F00398                     BC    15,STRT-4                                            ESCR4720
0475                            **        GENERAL RECOVERY PROCEDURE - PROCESSOR MODE                ESCR4730
0476    084C 498008BC           GRPM      CH    8,PSC1+2                                             ESCR4740
0477    0850 4700088C                     BC    0,RSIC              REISSUE SENSE INFORMATION COMMAND ESCR4750
0478    0854 92F00298                     MVI   SPSP+1,X'F0'                                         ESCR4760
0479    0858 91040205                     TM    OPT,4               ERROR PRINT OPTION?              ESCR4770
0480    085C 47100950                     BC    1,P*PR              PRINT ERROR                      ESCR4780
0481    0860 91080205                     TM    OPT,X'08'           OPT - BIT 4                      ESCR4790
0482    0864 47100896                     BC    1,ERCY-24                                            ESCR4800
0483    0868 47F005E0                     BC    15,SPM              RESUME PROCESSOR MODE            ESCR4810
0484                            **        GENERAL RECOVERY PROCEDURE - INPUT OUTPUT MODE             ESCR4820
0485    086C 498008BC           GRIO      CH    8,PSC1+2                                             ESCR4830
0486    0870 4720088C                     BC    2,RSIC              REISSUE SENSE INFORMATION COMMAND ESCR4840
0487    0874 92F002A8                     MVI   SPSI+1,X'F0'                                         ESCR4850
0488    0878 91040205                     TM    OPT,4               ERROR PRINT OPTION?              ESCR4860
0489    087C 47100950                     BC    1,P*PR              PRINT ERROR                      ESCR4870
0490    0880 91080205                     TM    OPT,X'08'                                            ESCR4880
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0491    0884 471088A6                   BC    1,ERCY-8                                          ESCR4890
0492    0888 47F088B2                   BC    15,RIOM          RESUME IO MODE                   ESCR4900
0493    088C AB880894           RSIC    SH    8,D16                                             ESCR4910
0494    0890 47F08080                   BC    15,0(,8)         REISSUE SENSE INFORMATION COMMAND ESCR4920
0495    0894 0010               D16     DC    X'0010'                                           ESCR4930
0496    0896 95830518                   CLI   XIOF+5,3         IF C2 OR C3 IN ERROR, DO NOT SET ESCR4940
0497    089A 472085E0                   BC    2,SPM            OPT BIT 4 SWITCH                 ESCR4950
0498    089E 928C08B5                   MVI   RIOM+3,X'0C'     SET RETURN TO GO TO COMMAND 2 - PM ESCR4960
0499    08A2 47F085E0                   BC    15,SPM                                            ESCR4970
0500    08A6 95830518                   CLI   XIOF+5,3         IF C2 OR C3 IN ERROR, DO NOT SET ESCR4980
0501    08AA 47208080                   BC    2,0(,8)          OPT BIT 4 SWITCH                 ESCR4990
0502    08AE 928C08B5           ERCY    MVI   RIOM+3,X'0C'     SET RETURN TO GO TO COMMAND 2 - IO ESCR5000
0503    08B2 47F08080           RIOM    BC    15,0(,8)                                          ESCR5010
0504    08B6 08AE               RIO     DC    Y(ERCY)                                           ESCR5020
0505    08B8 08A6               RPM     DC    Y(ERCY-8)                                         ESCR5030
0506    08BA 0000               PSC1    DC    X'0000'                                           ESCR5040
0507    08BC 0556                       DC    Y(INT)                                            ESCR5050
0508    08BE 0285               LIM1    DC    Y(C123+3)                                         ESCR5060
0509    08C0 0282                       DC    Y(C123)                                           ESCR5070
0510    08C2 0000               PSC2    DC    X'0000'                                           ESCR5080
0511    08C4 054E                       DC    Y(LOOP)                                           ESCR5090
0512    08C6 E0000CE0           IS      DC    X'E0000CE0'      INTERRUPT STATUS                 ESCR5100
0513    08CA 0000               DS      DC    X'0000'                                           ESCR5110
0514    08CC 0000               PSC3    DC    X'0000'          SET PM AND JUMP TO WHATEVER IR 8 ESCR5120
0515    08CE 08B2                       DC    Y(RIOM)          INDICATES                        ESCR5130
0516    08D0 0000               PSC4    DC    X'0000'          SET UP FOR SENSE INFORMATION     ESCR5140
0517    08D2 079A                       DC    Y(GSW)                                            ESCR5150
0518    08D4 0000               PSC5    DC    X'0000'                                           ESCR5160
0519    08D6 0398                       DC    Y(STRT-12)                                        ESCR5170
0520    08D8 0000               PSC6    DC    X'0000'                                           ESCR5180
0521    08DA 05EE                       DC    Y(UINT)                                           ESCR5190
0522    08DC 47000692           IOC     BC    0,TIO1                                            ESCR5200
0523    08E0 029A               YCP     DC    Y(SPSP)                                           ESCR5210
0524    08E2 02AA                       DC    Y(SPSI)                                           ESCR5220
0525    08E4 01F9               LDA     DC    Y(TM1)                                            ESCR5230
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0526                                *       *       *       *       *       *       *       * ESCR5248
0527                                *                                                       * ESCR5258
0528                                *                       PRINTOUT CONTROL ROUTINE        * ESCR5268
0529                                *     ENTRY * BAL  12,PRNT IN EITHER PROCESSOR OR I/O MODE * ESCR5278
0530                                *     EXIT  * IR 12 CONTAINS RETURN                     * ESCR5288
0531                                *     PRINTER ERROR * DISPLAY HALT = 3AAA, 3ESS, 3EEE   * ESCR5298
0532                                *           RECOVERY 1 ** CLEAR PRINTER FAULTS, START, RESUMES PRINT* ESCR5308
0533                                *           RECOVERY 2 ** ANALYZE STATUS. START REATTEMPTS PRINTING.* ESCR5318
0534                                *           RECOVERY 3 ** CLEAR P*01+5, START REATTEMPTS PRINTING.  * ESCR5328
0535                                *                       THIS STOP IS A CATASTROPHIC ERROR.        * ESCR5338
0536                                *       *       *       *       *       *       *       * ESCR5348
0537   08E6 470808F6                PRNT   BC    0,*+16                                      ESCR5358
0538   08EA A5030931                       TIO   PRDS+3,3          PRINTER AVAILABLE?        ESCR5368
0539   08EE 477A091A                       BC    7,P*08                                      ESCR5378
0540   08F2 92F808E7                       MVI   PRNT+1,X'F8'                                ESCR5388
0541   08F6 9201A058                       MVI   X'58',1            LOAD PRINTER BCW * PRINT AREA SET. ESCR5398
0542   08FA A4030811                       XIOF  X'11',3            PRINTER XIOF * NO INT. ALLOWED ESCR5408
0543   08FE 477808FA                       BC    7,*-4              PRINT XIOF NOT ACCEPTED. REISSUE. ESCR5418
0544   0902 A5030931                       TIO   PRDS+3,3          ACCEPTED. CHECK COMPLETION ESCR5428
0545   0906 472A0902                       BC    2,*-4                                       ESCR5438
0546   090A 47B80936                       BC    11,P*01                                     ESCR5448
0547   090E 95040931                       CLI   PRDS+3,4          DE SET?                   ESCR5458
0548   0912 4780C808                PEXT   BC    8,8(,12)           EXIT                   ESCR5468
0549   0916 47F0091E                       BC    15,*+8                                      ESCR5478
0550   091A 473A0936                P*08   BC    3,P*01                                      ESCR5488
0551   091E 95808931                       CLI   PRDS+3,X'80'                                ESCR5498
0552   0922 477A092E                       BC    7,*+12                                      ESCR5508
0553   0926 A9083AAA                       HPR   X'3AAA'             PRINTER ABNORMAL. CORRECT. ESCR5518
0554   092A 47F808EA                       BC    15,PRNT+4           TO RESUME, START        ESCR5528
0555   092E A9083E80                PRDS   HPR   X'3E80'             PRINTER ERROR. DISPLAY '3ESS' WHERE ESCR5538
0556   0932 47F808EA                       BC    15,PRNT+4           SS = STORED STATUS. CORRECT ERROR. ESCR5548
0557                                *                                 START RESUMES PRINTING. ESCR5558
0558   0936 A9083EEE                P*01   HPR   X'3EEE'             CATASTROPHIC PRINTER ERROR ESCR5568
0559   093A 47F80936                       BC    15,P*01                                     ESCR5578
0560   093E 47F808EA                       BC    15,PRNT+4                                   ESCR5588
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0561  0942 92000080      CPAR   MVI   X'80',0              CLEAR PRINTER AREA          ESCR5590
0562  0946 D2820081008D         MVC   X'81'(131),X'80'                                 ESCR5600
0563  094C 47F0C000             BC    15,0(,12)                                        ESCR5610
0564  0950 47000962      P*PR   BC    0,*+18                                           ESCR5620
0565  0954 D2830008008D2        MVC   X'80'(132),PHD1                                  ESCR5630
0566  095A 45C008E6             BAL   12,PRNT                                          ESCR5640
0567  095E 92F00951             MVI   *-13,X'F0'                                       ESCR5650
0568  0962 45C00942             BAL   12,CPAR                                          ESCR5660
0569  0966 48E00C78             LH    14,P*T               FORMAT 1                  ESCR5670
0570  096A 95600AFF             CLI   EMX+5,X'60'          UNISERVO 6-C'S ARE BEING USED ESCR5680
0571  096E 47800AE6             BC    8,E6CD                                           ESCR5690
0572  0972 91800285             TM    OPT,X'80'             EDIT RECORDING DENSITY     ESCR5700
0573  0976 47100AF0             BC    1,EDD                                            ESCR5710
0574  097A D2040085C5D          MVC   X'85'(5),DEN+7        PHASE                      ESCR5720
0575  0980 F384008E053E  EDI    UNPK  X'8E'(9),XIO(5)       EDIT INSTRUCTION           ESCR5730
0576  0986 DC07008EE000         TR    X'8E'(8),0(14)                                   ESCR5740
0577  098C 9240096             MVI   X'96',X'40'                                      ESCR5750
0578  0990 45C00B6E             BAL   12,EDS               EDIT DEVICE STATUS         ESCR5760
0579  0994 91800053F            TM    XIO+1,X'80'           MX OR SEL                  ESCR5770
0580  0998 47100AFA             BC    1,EMX                                            ESCR5780
0581  099C 91200053F            TM    XIO+1,X'20'                                      ESCR5790
0582  09A0 47800AFA             BC    8,EMX                                            ESCR5800
0583  09A4 F3E700A50078         UNPK  X'A5'(15),X'78'(8)  EDIT 78-7F                   ESCR5810
0584  09AA F32100B3007F         UNPK  X'B3'(3),X'7F'(2)                                ESCR5820
0585  09B0 DC0F00A5E000         TR    X'A5'(16),0(14)                                  ESCR5830
0586  09B6 92400085             MVI   X'B5',X'40'                                      ESCR5840
0587  09BA D501051A0C62         CLC   XIOF+4(2),C1AD                                   ESCR5850
0588  09C0 47800B46             BC    8,ESC1                                           ESCR5860
0589  09C4 D501051A0C64         CLC   XIOF+4(2),C2AD                                   ESCR5870
0590  09CA 47800B56             BC    8,ESC2                                           ESCR5880
0591  09CE F3E700B60228         UNPK  X'B6'(15),CW3(8)    EDIT SELECTOR COMMAND WORD 3 ESCR5890
0592  09D4 F32100C4022F         UNPK  X'C4'(3),CW3+7(2)                                ESCR5900
0593  09DA DC0F00B6E000         TR    X'B6'(16),0(14)                                  ESCR5910
0594  09E0 92400C6              MVI   X'C6',X'40'                                      ESCR5920
0595  09E4 91100285             TM    OPT,X'10'             EDIT SIMULATE              ESCR5930
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0596   09E8 471009B6          BC    1,ESY                                    ESCR5940
0597   09EC 92D500F8          MVI   X'F8',X'D5'      N - SIMULATION NOT SET   ESCR5950
0598   09F0 9503053F  EGS     CLI   XIO+1,3          GET SENSE INFORMATION?   ESCR5960
0599   09F4 47C00ADE          BC    12,SIDR                                  ESCR5970
0600   09F8 92F00831          MVI   PRSW+1,X'F8'                             ESCR5980
0601   09FC 912000B5          TM    OPT,X'20'        IO OR PM                ESCR5990
0602   0A00 4710079A          BC    1,GSW                                    ESCR6000
0603   0A04 47F0078E          BC    15,GSW-12                                ESCR6010
0604   0A08 48E00C78          LH    14,P*T                                   ESCR6020
0605   0A0C 92000831          MVI   PRSW+1,0                                 ESCR6030
0606   0A10 F3A500D900268     UNPK  X'D9'(11),NSNS(6)  EDIT NORMAL SENSE     ESCR6040
0607   0A16 F3A500E4026D      UNPK  X'E4'(11),MSNS(6)  EDIT MONITOR SENSE    ESCR6050
0608   0A1C DC1400D9E000      TR    X'D9'(21),0(14)                          ESCR6060
0609   0A22 92400E3           MVI   X'E3',X'40'                              ESCR6070
0610   0A26 92400EE           MVI   X'EE',X'40'                              ESCR6080
0611   0A2A 45C00E6           BAL   12,PRNT                                  ESCR6090
0612   0A2E 47F00A82  SSBE    BC    15,BSMD-38       SENSE BYTE-BIT-EDIT SWITCH ESCR6100
0613   0A32 48D00246          LH    13,BCW4+2                                ESCR6110
0614   0A36 48E00956          LH    14,P*PR+6                                ESCR6120
0615   0A3A 48F00E1E          LH    15,YS0                                   ESCR6130
0616   0A3E 45C00942          BAL   12,CPAR                                  ESCR6140
0617   0A42 D2000A4900EC9     MVC   TMI+1(1),TMT                             ESCR6150
0618   0A48 91800D00          TM    0(13),X'80'                              ESCR6160
0619   0A4C 47100AA8          BC    1,BSMD           BIT N SET, STORE ASSOCIATED MESSAGE ESCR6170
0620   0A50 A6010A46          AI    TMI-2,1                                  ESCR6180
0621   0A54 AAF00244          AH    15,BCW4                                  ESCR6190
0622   0A58 95010A49          CLI   TMI+1,X'01'      8 BITS OF THIS BYTE TESTED? ESCR6200
0623   0A5C 47800A64          BC    8,*+8                                    ESCR6210
0624   0A60 47F00A42          BC    15,TMI-6         TEST NEXT BIT           ESCR6220
0625   0A64 AAD00272          AH    13,D1                                    ESCR6230
0626   0A68 49D00ED4          CH    13,LNS           10 BYTES OF SENSE TESTED? ESCR6240
0627   0A6C 47800A7A          BC    8,*+14           PRINT STORED MESSAGES   ESCR6250
0628   0A70 D2010A4600ED2     MVC   TMI-2(2),YTMT    RESET BIT TABLE         ESCR6260
0629   0A76 47F00A42          BC    15,TMI-6         TEST BIT 0 OF NEXT SENSE BYTE ESCR6270
0630   0A7A 92F00A2F          MVI   SSBE+1,X'F8'      RESET SENSE BYTE-BIT-EDIT SWITCH ESCR6280
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0631  0A7E 45C0 08E6                BAL   12,PRNT             PRINT MESSAGES                ESCR6290
0632  0A82 45C0 0942                BAL   12,CPAR                                         ESCR6300
0633  0A86 45C0 08E6                BAL   12,PRNT                                         ESCR6310
0634  0A8A D201 0A46 0ED2           MVC   TMI-2(2),YTMT                                   ESCR6320
0635  0A90 9200 029B                MVI   SPSP+1,0                                        ESCR6330
0636  0A94 9200 02AB                MVI   SPSI+1,0                                        ESCR6340
0637  0A98 9108 0285                TM    OPT,X'08'                                       ESCR6350
0638  0A9C 4710 08AE                BC    1,ERCY                                          ESCR6360
0639  0AA0 4700 0ACE                BC    0,IRCY                                          ESCR6370
0640  0AA4 47F0 8000                BC    15,0(,8)            RESUME                      ESCR6380
0641  0AA8 D204 E000 F000           MVC   0(5,14),0(15)                                   ESCR6390
0642  0AAE AAE0 0244                AH    14,BCW4             INCR. PRINTER AREA          ESCR6400
0643  0AB2 49E0 0ED6                CH    14,LPA              ALL PRINTER AREA FILLED?    ESCR6410
0644  0AB6 4780 0ABE                BC    8,*+8               PRINT                       ESCR6420
0645  0ABA 47F0 0A50                BC    15,TMI+8            GET REMAINING MESSAGES      ESCR6430
0646  0ABE 45C0 08E6                BAL   12,PRNT                                         ESCR6440
0647  0AC2 45C0 0942                BAL   12,CPAR                                         ESCR6450
0648  0AC6 48E0 0956                LH    14,P+PR+6           RESET IR14                  ESCR6460
0649  0ACA 47F0 0A50                BC    15,TMI+8                                        ESCR6470
0650  0ACE 9120 0285      IRCY      TM    OPT,X'20'           PM OR IO?                   ESCR6480
0651  0AD2 9200 0AA1                MVI   BSMD-7,0                                        ESCR6490
0652  0AD6 4710 8000                BC    1,0(,8)                                         ESCR6500
0653  0ADA 47F0 05E0                BC    15,SPM                                          ESCR6510
0654  0ADE 92F0 0AA1      SIDR      MVI   BSMD-7,X'F0'        SET INTERNAL DEVICE RECOVERY ESCR6520
0655  0AE2 47F0 0A7E                BC    15,BSMD-42                                      ESCR6530
0656  0AE6 D203 0085 0C56 E6CD      MVC   X'85'(4),DEN                                    ESCR6540
0657  0AEC 47F0 0980                BC    15,EDI                                          ESCR6550
0658  0AF0 D206 0085 0C56 EDD       MVC   X'85'(7),DEN         NRZI                       ESCR6560
0659  0AF6 47F0 0980                BC    15,EDI                                          ESCR6570
0660  0AFA F384 00C7 00F0 EMX       UNPK  X'C7'(9),X'70'(5)   EDIT TERMINATION BCW       ESCR6580
0661  0B00 DC07 00C7 E000           TR    X'C7'(8),0(14)                                  ESCR6590
0662  0B06 9240 00CF                MVI   X'CF',X'40'                                     ESCR6600
0663  0B0A D501 051A 0C62           CLC   XIOF+4(2),C1AD                                  ESCR6610
0664  0B10 4780 0B32                BC    8,EMC1                                          ESCR6620
0665  0B14 D501 051A 0C64           CLC   XIOF+4(2),C2AD                                  ESCR6630
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0666     0B1A 47800B3C                      BC    8,EMC2                                        ESCR6640
0667     0B1E F38400D0020E                  UNPK  X'D0'(9),BCW3(5)                              ESCR6650
0668     0B24 DC0700D0E000                  TR    X'D0'(8),0(14)                                ESCR6660
0669     0B2A 924000D8                      MVI   X'D8',X'40'                                   ESCR6670
0670     0B2E 47F009E4                      BC    15,ECC+10                                     ESCR6680
0671     0B32 F38400D00206         EMC1     UNPK  X'D0'(9),BCW1(5)                              ESCR6690
0672     0B38 47F00B24                      BC    15,EMC1-14                                    ESCR6700
0673     0B3C F38400D0020A         EMC2     UNPK  X'D0'(9),BCW2(5)                              ESCR6710
0674     0B42 47F00B24                      BC    15,EMC1-14                                    ESCR6720
0675     0B46 F3E700B60218         ESC1     UNPK  X'B6'(15),CW1(8)    EDIT SELECTOR COMMAND WORD1   ESCR6730
0676     0B4C F32100C4021F                  UNPK  X'C4'(3),CW1+7(2)                             ESCR6740
0677     0B52 47F009DA                      BC    15,ECC                                        ESCR6750
0678     0B56 F3E700B60220         ESC2     UNPK  X'B6'(15),CW2(8)    EDIT SELECTOR COMMAND WORD 2  ESCR6760
0679     0B5C F32100C40227                  UNPK  X'C4'(3),CW2+7(2)                             ESCR6770
0680     0B62 47F009DA                      BC    15,ECC                                        ESCR6780
0681     0B66 92E800F0             ESY      MVI   X'F0',X'E8'         Y - SIMULATION IS SET     ESCR6790
0682     0B6A 47F009F0                      BC    15,EGS                                        ESCR6800
0683     0B6E 48E00C78             EDS      LH    14,P*T                                        ESCR6810
0684     0B72 F38400990040                  UNPK  X'99'(9),X'40'(5)   EDIT 40-43                ESCR6820
0685     0B78 DC070099E000                  TR    X'99'(8),0(14)                                ESCR6830
0686     0B7E 924000A1                      MVI   X'A1',X'40'                                   ESCR6840
0687     0B82 F32100A200CA                  UNPK  X'A2'(3),DS(2)      EDIT DS                   ESCR6850
0688     0B88 DC0100A2E000                  TR    X'A2'(2),0(14)                                ESCR6860
0689     0B8E 924000A4                      MVI   X'A4',X'40'                                   ESCR6870
0690     0B92 47F0C000                      BC    15,0(,12)                                     ESCR6880
0691     0B96 91800205             E46C     TM    OPT,X'80'          NRZI?                      ESCR6890
0692     0B9A 478007D4                      BC    8,GMS                                         ESCR6900
0693     0B9E D2130D650E93                  MVC   M0+15(20),N6CE                                ESCR6910
0694     0BA4 D2040DAB0EA7                  MVC   M0+85(5),N6CE+20                              ESCR6920
0695     0BAA D2040DBF0DB5                  MVC   M0+105(5),M0+95                               ESCR6930
0696     0BB0 D2040DB50EAC                  MVC   M0+95(5),N6CE+25                              ESCR6940
0697     0BB6 D2270DC40E3E                  MVC   M0+110(40),NESI+30                            ESCR6950
0698     0BBC D2040DEC0E39                  MVC   M0+150(5),NESI+25                             ESCR6960
0699     0BC2 D2270DF10E6B                  MVC   M0+155(40),NESI+75                            ESCR6970
0700     0BC8 D2040E190E66                  MVC   YS0-5(5),NESI+70                              ESCR6980
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0701    0BCE 47F007D8                          BC    15,GMS+4                                          ESCR6990
0702    0BD2 C5E2C3D940C4C5D5E2C9E3E840C9D5E2 PHD1  DC    C'ESCR DENSITY INS'      PRINT HEADER 1           ESCR7000
0703    0BE2 E3D9E4C3E3C9D6D540F4F0F4F1F4F2F4       DC    C'TRUCTION 4041424'                               ESCR7010
0704    0BF2 F340C4E240F7F8F7F9F7C1F7C2F7C3F7       DC    C'3 DS 78797A7B7C7'                               ESCR7020
0705    0C02 C4F7C5F7C640C3D6D4C4C2C1C4D9C6D3       DC    C'D7E7F COMDBADRFL'                               ESCR7030
0706    0C12 C1C7C2C3D5E340E3C5D9D460C2C3E640       DC    C'AGBCNT TERM-BCW '                               ESCR7040
0707    0C22 C9D5C9E360C2C3E640E2F0E2F1E2F2E2       DC    C'INIT-BCW S0S1S2S'                               ESCR7050
0708    0C32 F3E2F440D4F0D4F1D4F2D4F3D4F440E2       DC    C'3S4 M0M1M2M3M4 S'                               ESCR7060
0709    0C42 C9D4404040404040404040404040404040     DC    C'IM                '                             ESCR7070
0710    0C52 40404040                              DC    C'    '                                           ESCR7080
0711    0C56 D5D9E9C940C3C2D7C8C1E2C5          DEN  DC    C'NRZI CBPHASE'                                   ESCR7090
0712    0C62 0203                              C1AD DC    Y(C123+1)                                         ESCR7100
0713    0C64 0204                              C2AD DC    Y(C123+2)                                         ESCR7110
0714    0C66 00000000                          EBCW DC    X'00000000'                                       ESCR7120
0715    0C6A F6C34040F74040F8F0F0404040D5      SHDC DC    C'6C  7  800  N'                                  ESCR7130
0716    0C78 0B8A                              P*T  DC    Y(*+2-240)                                        ESCR7140
0717    0C7A F0F1F2F3F4F5F6F7F8F9C1C2C3C4C5C6       DC    CL16'0123456789ABCDEF'                            ESCR7150
0718    0C8A 0826                              ARSM DC    Y(RSIM+10)                                        ESCR7160
0719    0C8C 041A                                   DC    Y(SPC)                                            ESCR7170
0720    0C8E C3D4D9D140C9D5D9D840C2E2C3D240    S0   DC    C'CMRJ INRQ BSCK '  SENSE BYTE ZERO             ESCR7180
0721    0C9D C5D8C3D240C4C1C3D240D6E5D9D540         DC    C'EQCK DACK OVRN '                                ESCR7190
0722    0CAC E6C4C3E940E2C2F0F740                   DC    C'WDCZ SB07 '                                     ESCR7200
0723    0CB6 D5D6C9E240E3E4E2C140E3E4E2C240         DC    C'NOIS TUSA TUSB ' SENSE BYTE ONE                 ESCR7210
0724    0CC5 F7E3D9D240C2D6E34040C5D6E34040         DC    C'7TRK BOT  EOT  '                                ESCR7220
0725    0CD4 E3E4C6D740E3E4C9C340                   DC    C'TUFP TUIC '                                     ESCR7230
0726    0CDE E3C9C5F040E3C9C5F140E3C9C5F240         DC    C'TIE0 TIE1 TIE2 ' SENSE BYTE TWO                 ESCR7240
0727    0CED E3C9C5F340E3C9C5F440E3C9C5F540         DC    C'TIE3 TIE4 TIE5 '                                ESCR7250
0728    0CFC E3C9C5F640E3C9C5F740                   DC    C'TIE6 TIE7 '                                     ESCR7260
0729    0D06 E5D9C34040D4C4E34040E2D2C5E640         DC    C'VRC  MDT  SKEW ' SENSE BYTE THREE               ESCR7270
0730    0D15 D7E2E3C340E2C4E34040E3E4D7C840         DC    C'PSTC SDT  TUPH '                                ESCR7280
0731    0D24 C2D2E6C440E2C2F3F740                   DC    C'BKWD SB37 '                                     ESCR7290
0732    0D2E D9E6C1E840E3D4C6E340E2C2F4F240         DC    C'RWAY TMFT SB42 ' SENSE BYTE FOUR                ESCR7300
0733    0D3D E2C2F4F340E2C2F4F440E2E3C1D340         DC    C'SB43 SB44 STAL '                                ESCR7310
0734    0D4C E3D7C6E340E2C2F4F740                   DC    C'TPFT SB47 '                                     ESCR7320
0735    0D56 D7C3F0F040D7C3F0F140D7C3F0F240    M0   DC    C'PC00 PC01 PC02 ' MONITOR SENSE BYTE ZERO        ESCR7330
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0736  0D65 F6C1E54040F7C1E54040F8C1E54040          DC    C'6AV  7AV  8AV  '                                  ESCR7340
0737  0D74 D9C5E24040E2C9D44040                    DC    C'RES  SIM  '                                       ESCR7350
0738  0D7E E6D9C9E340D9C5C1C440C2D2E6C440          DC    C'WRIT READ BKWD ' MONITOR SENSE BYTE ONE           ESCR7360
0739  0D8D E2D7C1C340C6C9D3C540D9C5E64040          DC    C'SPAC FILE REW  '                                  ESCR7370
0740  0D9C E6E3D44040C5D9C1E240                    DC    C'WTM  ERAS '                                       ESCR7380
0741  0DA6 D7D9C5D940E2C5D5E340E3D4C44040          DC    C'PRER SENT TMD  '  MONITOR SENSE BYTE TWO          ESCR7390
0742  0DB5 D7E2E3C140C3E3D9D440D4D9D7C840          DC    C'PSTA CTRM MRPH '                                  ESCR7400
0743  0DC4 C4E3D74040C4E3F04040                    DC    C'DTP  DT0  '                                       ESCR7410
0744  0DCE C4E3F14040C4E3F24040C4E3F34040          DC    C'DT1  DT2  DT3  ' MONITOR SENSE BYTE THREE         ESCR7420
0745  0DDD C4E3F44040C4E3F54040C4E3F64040          DC    C'DT4  DT5  DT6  '                                  ESCR7430
0746  0DEC C4E3F74040D7E9C5D740                    DC    C'DT7  PZEP '                                       ESCR7440
0747  0DF6 D7E9C5F040D7E9C5F140D7E9C5F240          DC    C'PZE0 PZE1 PZE2 ' MONITOR SENSE BYTE FOUR          ESCR7450
0748  0E05 D7E9C5F340D7E9C5F440D7E9C5F540          DC    C'PZE3 PZE4 PZE5 '                                  ESCR7460
0749  0E14 D7E9C5F640D7E9C5F740                    DC    C'PZE6 PZE7 '                                       ESCR7470
0750  0E1E 0C8E                              YS0   DC    Y(S0)                                               ESCR7480
0751  0E20 C4C3C3D240D9E5D9C340D3D9C34040    NESI  DC    C'DCCK RVRC LRC  ' NRZI EDITED SENSE INFORMATION   ESCR7490
0752  0E2F C3D9C34040E6E5D9C340C3D9C3D740          DC    C'CRC  WVRC CRCP '                                  ESCR7500
0753  0E3E C3D9C3F040C3D9C3F140C3D9C3F240          DC    C'CRC0 CRC1 CRC2 '                                  ESCR7510
0754  0E4D C3D9C3F340C3D9C3F440C3D9C3F540          DC    C'CRC3 CRC4 CRC5 '                                  ESCR7520
0755  0E5C C3D9C3F640C3D9C3F740D3D9C3D740          DC    C'CRC6 CRC7 LRCP '                                  ESCR7530
0756  0E6B D3D9C3F040D3D9C3F140D3D9C3F240          DC    C'LRC0 LRC1 LRC2 '                                  ESCR7540
0757  0E7A D3D9C3F340D3D9C3F440D3D9C3F540          DC    C'LRC3 LRC4 LRC5 '                                  ESCR7550
0758  0E89 D3D9C3F640D3D9C3F740                    DC    C'LRC6 LRC7 '                                       ESCR7560
0759  0E93 C4C5D5F040C4C5D5F140C5D7C1D940    N6CE  DC    C'DEN0 DEN1 EPAR ' NRZI 6C EDITED SENSE INFORMATION ESCR7570
0760  0EA2 C4C3D6D540C5C7C1D740D3D6E6C740          DC    C'DCON EGAP LOWG '                                  ESCR7580
0761  0EB1 E4D5E2D6D3C9C3C9E3C5C440C9D5E3C5  EUI   DC    C'UNSOLICITED INTE'                                 ESCR7590
0762  0EC1 D9D9E4D7E3405C5C                        DC    C'RRUPT **'                                         ESCR7600
0763  0EC9 8040201008040201                  TMT   DC    X'8040201008040201' TEST MASK TABLE                 ESCR7610
0764  0ED2 0EC9                              YTMT  DC    Y(TMT)                                              ESCR7620
0765  0ED4 0272                              LNS   DC    Y(NSNS+10)                                          ESCR7630
0766  0ED6 00F8                              LPA   DC    X'00F8'                                             ESCR7640
0767  0ED8                                   SPA   DS    1CL132                                              ESCR7650
0768  0020                                        ORG   X'20'       REVISION LEVEL TO 0020                  ESCR7660
0769  0020 FF                                REV   DC    X'FF'                                               ESCR7670
0770       00003000034A                           END   CKPC                                                  ESCR7680
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